

Exhibit 1

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Mark Birrittella
Development Building
Cray Research, Inc.
900 Lowater Road
Chippewa Falls, WI 54729

Re: Technology Review Presentation Materials

Dear Mark:

A copy of the presentation materials from the **REDACTED** technology review is enclosed for use by Cray Research, Inc. in accordance with that certain License Agreement between MicroUnity Systems Engineering, Inc. and Cray Research Inc. dated **REDACTED**. Under this agreement, Cray has an obligation to protect information disclosed pursuant to the agreement which is "in written, graphic, machine readable or other tangible form and is conspicuously marked 'Confidential', 'Proprietary' or in some other manner to indicate its confidential nature." The quarterly review presentation materials are confidential information.

Please contact me upon your receipt of this letter to verify proper delivery of the materials. I may be reached at (408) 734-8100.

Sincerely,



Tim Robinson
Director of Systems Engineering

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Enclosure: Copy of the **REDACTED** technology review presentation materials

cc: John Moussouris, MicroUnity Systems Engineering, Inc.

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Agenda for the Cray Research and MicroUnity Review

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Tuesday

- 2.00 PM Introduction
- 2.15 PM Process Status
Paul Poenisch
- 4.00 PM Split for Business Meeting
Discussion

Wednesday

- 8.00 AM Architecture Update
Craig Hansen
Tom Karzes
- 10.00 AM Circuits Update
Bill Herndon
Geert Rosseel
- 11.00 AM Euterpe Implementation
Geert Rosseel
Tim Robinson
- 12.00 PM Lunch - Discussion
- 1.00 PM Meeting Concludes

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MicroUnity I.C. Process Status

Agenda

- Introduction - process overview
- Historical perspective
- Current facility and equipment status
- Process status
- Current Device Status
- Documentation
- Summary

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MicroUnity I.C. Process Status

Key Features of MOBI MOS 1

- 0.5 micron line and space on all layers.
- Advanced, non phase shifting, reticles.
- Maximum non-planarity at photomasking and metal deposition of < 0.15 microns.
- Four routing layers of metal, top two are air bridged.
- Symmetric PMOS and NMOS transistors.
- F_t of bipolar transistors > 40 GHz.

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Key Features of MOBI MOS 1 (continued)

- Package consists of die, space transformer and TAB.
- Metallization is inherently electromigration resistant.

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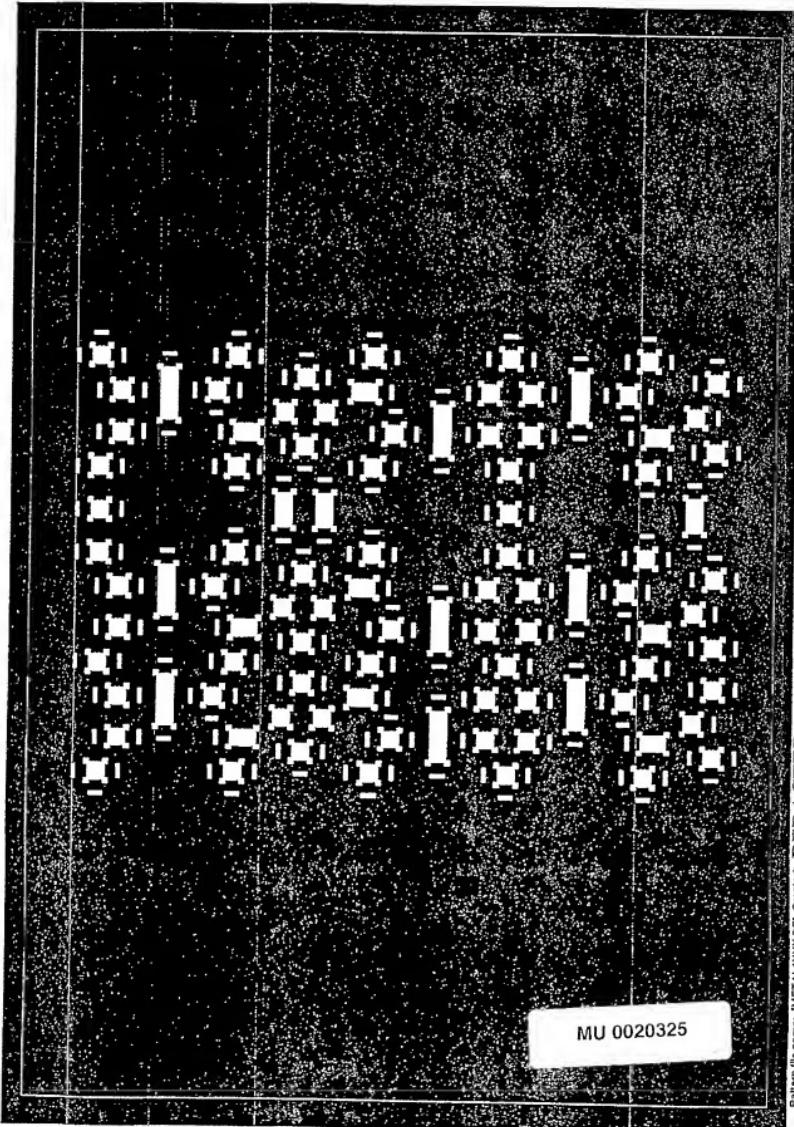
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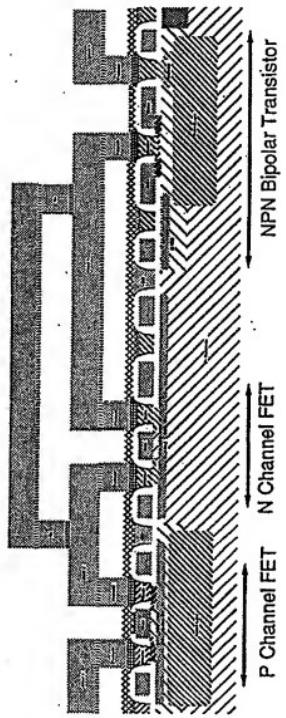


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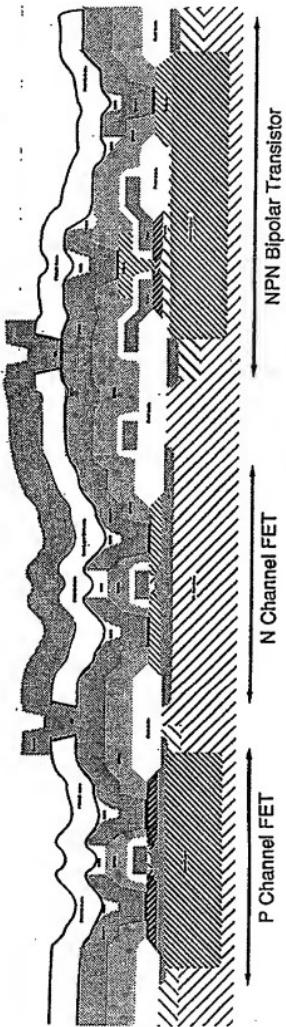
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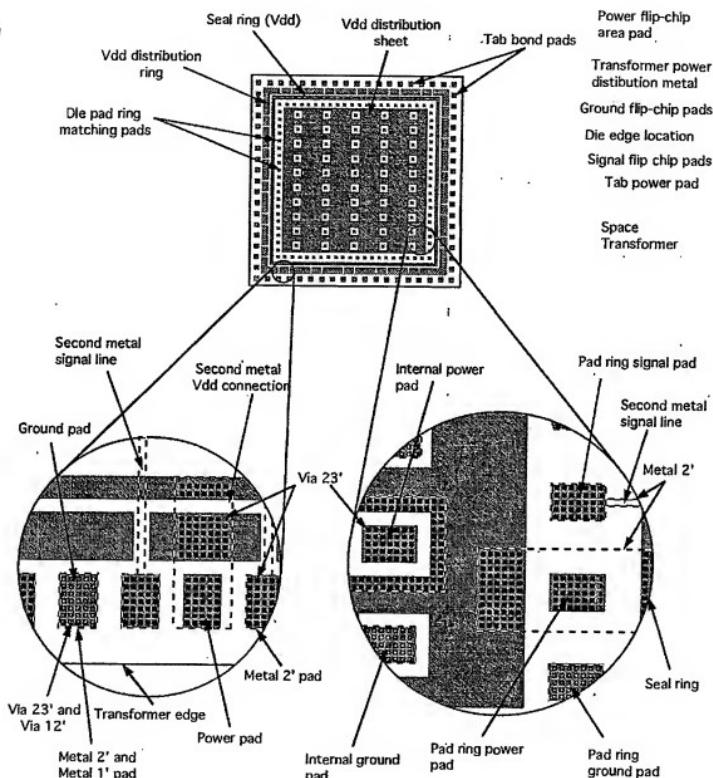
MicroUnity BiCMOS Process Cross Section



Conventional BiCMOS Process Cross Section



Space Transformer Layout

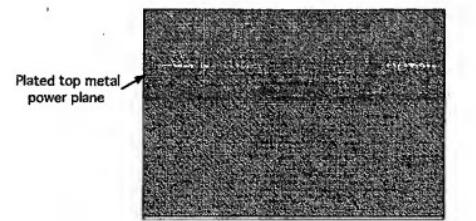
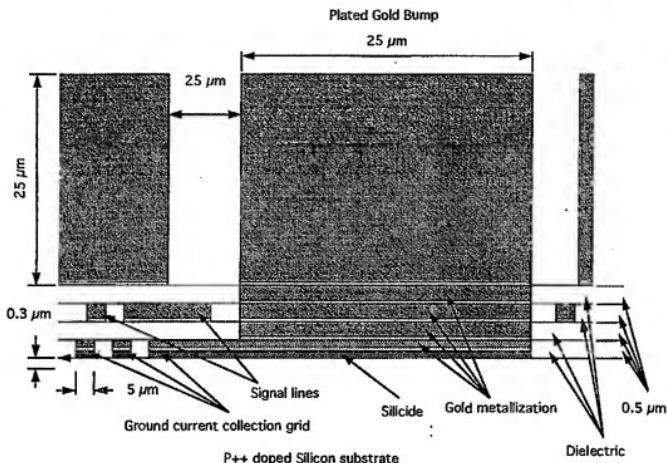


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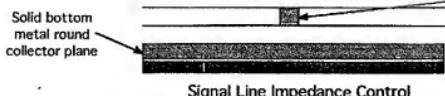
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Space Transformer Structure



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Vendor	Digital CMOS-5	Fujitsu CS-50	HP CMOS-14	IBM CMOS-6S	Intel CMOS-5X	Ti "0.6 micron"	TI EPIC-2BE	MicroUnity EPIC-3	MicroUnity MPBMCs
Example Product	21064A	Sparc-2	PA-7200	PPC 620	PPO 6014	P54C	SSparc	MVP	Calloope
First Production	3Q94	1Q94	4Q94	4Q94	4Q94	1Q94	2Q94	3Q94	4Q94
Supply Voltage	3.3 V	3.3 V	4.4 V	3.3 V	2.5 V	3.3 V	4.8 V	3.3 V	3.3 V
BCMOS?	no	no	no	no	no	yes	yes	opt	yes
Gate Length; Drawn (microns)	0.50	0.50	0.55	0.50	0.50	0.50	0.60	0.55	0.50
Gate Length; Effective (microns)	0.37	0.45	0.38	0.39	0.25	0.37	0.50	0.47	0.35
Gate Oxide Thickness (angstroms)	9.0	11.0	12.0	9.0	7.0	8.0	12.0	9.0	10.8
No. of Metal Layers	4	3 - 4	3	5	5	4	3	3 - 4	5
Local Interconnect?	yes	no	no	yes	yes	no	yes	no	yes
Stacked Vias?	no	no	no	yes	yes	no	yes	yes	yes
M1 contacted pitch (microns)	1.5	2.1	1.8	1.4	1.2	1.4	2.0	1.8	1.0
M2 contacted pitch (microns)	1.8	2.1	1.8	1.8	1.8	1.7	2.0	1.8	1.0
M3 contacted pitch (microns)	5.0	2.1	2.4	1.8	1.8	1.7	2.6	2.4	1.0
M4 contacted pitch (microns)	5.0	21.0	-	1.8	1.8	3.5	-	4.0	1.0
Routing Index (square microns)	4.9	4.4	4.3	2.7	2.5	2.9	4.3	4.1	0.8

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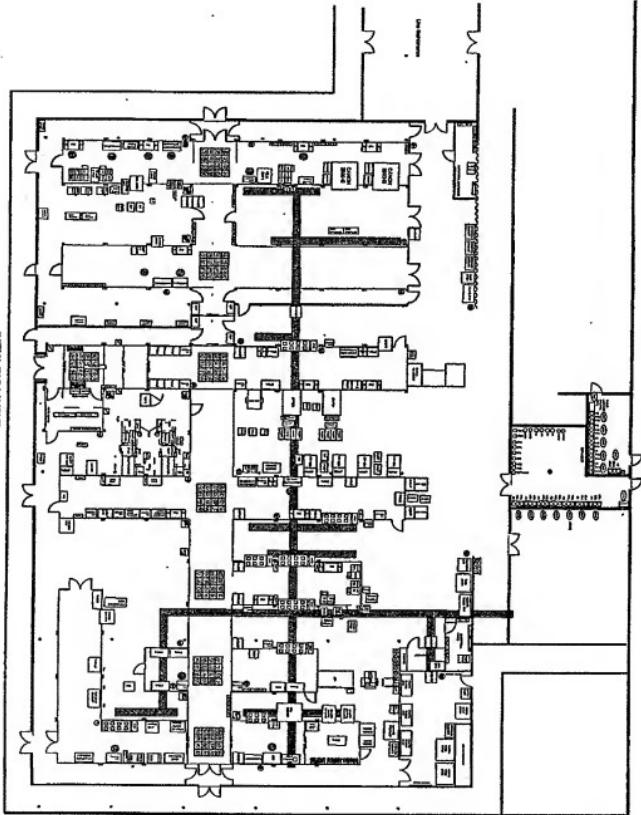
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INITIAL FAB LAYOUT
REV. A



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MicroUnity Systems Engineering, Inc. REDACTED Process Status Review

MicroUnity I.C. Process Status

Historical perspective on MicroUnity's I.C. Fab

■ Time line of events

'93-'94 month	J	J	A	S	O	N	D	J	F	M	A	M	J	J	A	S	O	N	D
Const. Go-ahead	▼																		
Ground Braking	▼																		
1st. Equip. Ord.	▼																		
Facilities Comp.	▼																		
1st Equip. Del.	▼																		
Last Proc. Eq.	▼																		
Last Pack. Eq.	▼																		
Start 1st Test.	▼																		
Start 1st Prod.	▼																		
1st Transistors	▼																		
1st lot out	▼																		
1st Yielding Part	▼																		
1st Pack. Parts	▼																		

MicroUnity I.C. Process Status

MicroUnity Fab current status

■ Facilities

- The fab was designed to provide a cleanliness level of class 10 or better.

Currently the fab is running below the class 1 level 95% of the time with occasional excursions to ~ class 10.

- Facilities are 95% built out, 100% by December.
- Temperature tracking +/- 0.25 F.
- Humidity tracking +/- 1% RH.

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MicroUnity Fab current status (continued)

■ Equipment

— Photomasking

One i-line stepper in production operation

One i-line stepper in qualification

Resist spin coat capacity adequate for pilot operations

One additional develop track on order.

— Etch/PECVD/Ion implant

Two plasma etch systems (ten chambers) and one
PECVD system (5 chambers) are in production operation

One medium current implanter is in production operation.

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MicroUnity Fab current status (continued)

■ Equipment (continued)

— Metallization

Two metal evaporators (six pockets each) are in production operation

One lift-off tool is being characterized by engineering and one is waiting bring-up

Two plating stations are up and running (three tanks each, one in use, one ready for fill).

— Diffusion and Epi

Seven vertical diffusion tubes have processes up and running on them and, six have been released to production

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MicroUnity Fab current status (continued)

■ Equipment (continued)

— Diffusion and Epi (continued)

One epi system is up and released to production for the thin epi layer, thick layer is in engineering evaluation.

— Packaging

Wafer saw, sawed wafer cleaner, wafer mounting station and developmental flip-chip bonder have been released to production.

TAB bonder, and airbridge equipment are in engineering evaluation.

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MicroUnity I.C. Process Status

Process Status

■ Transistors

- There are several critical alignments in the formation of the transistors (Bipolar and MOS). To date alignment on our single production stepper has been within the 3 sigma plus offset requirement, <0.15.
 - “Poly waffilization” is the method chosen to maintain planarity and CD control at gate/base formation.
 - CD is being gathered now and so far looks good, but more data is needed
- Layout was not adversely effected, SRAM cell is 22 sq. microns, the ECL atom is 96 sq. microns.

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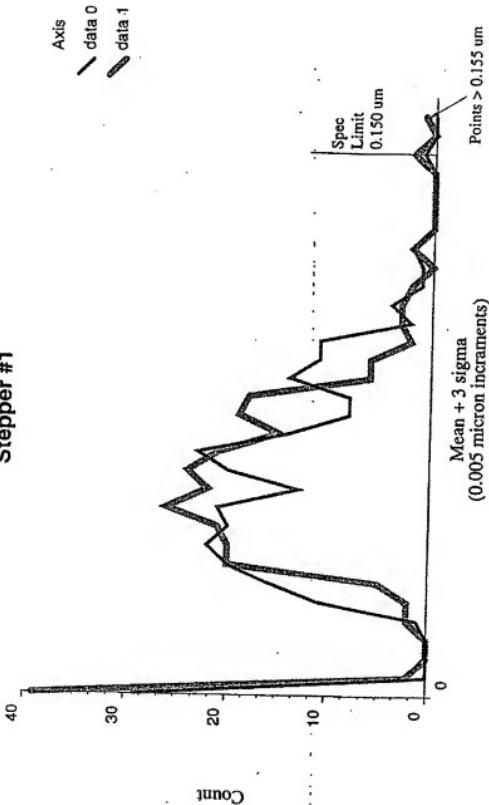
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Alignment History

Mean + 3 Sigma Alignment

Stepper #1



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Process Status (continued)

■ Transistors (continued)

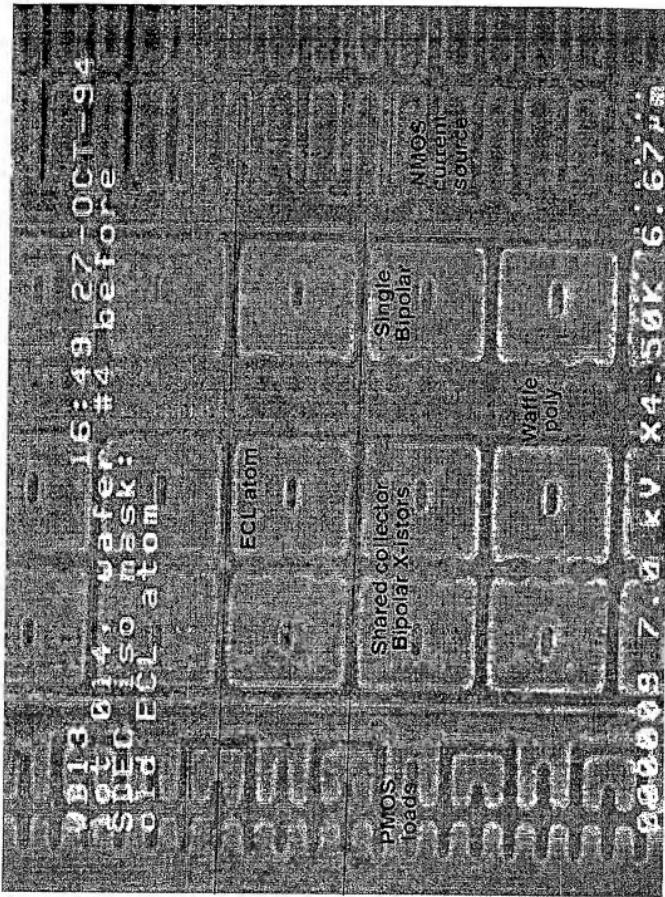
- Source, drain, emitter and collector areas are extended vertically by polysilicon formation between the poly 1 features (SDEC)
SDEC formation is doable but more work is needed.
- Silicide used is CoSi_2
Silicide appears to be stable with the metal system in use.
- No testable transistors have reached E-test yet, we expect this to occur within two weeks.

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ECL Atoms



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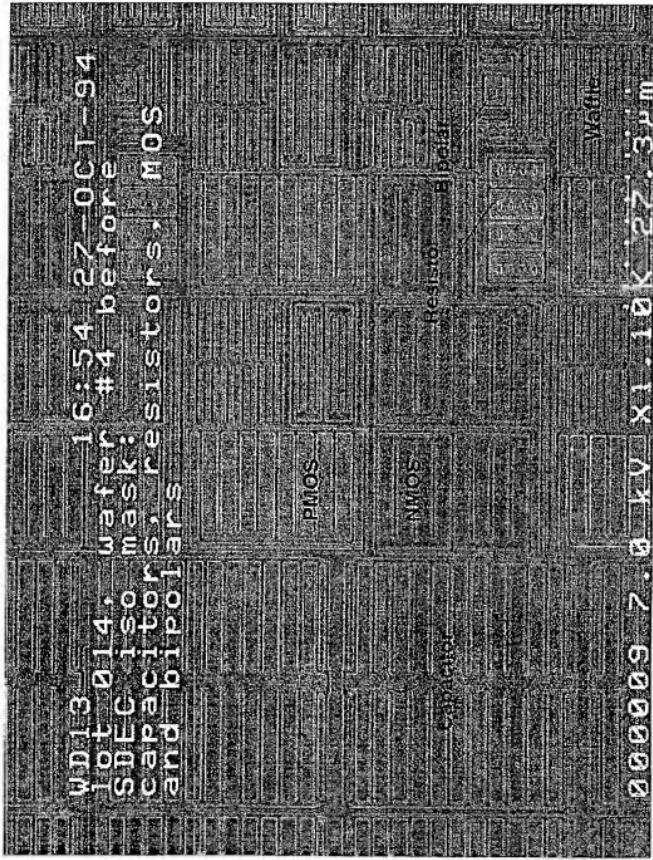
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Analog Device Section

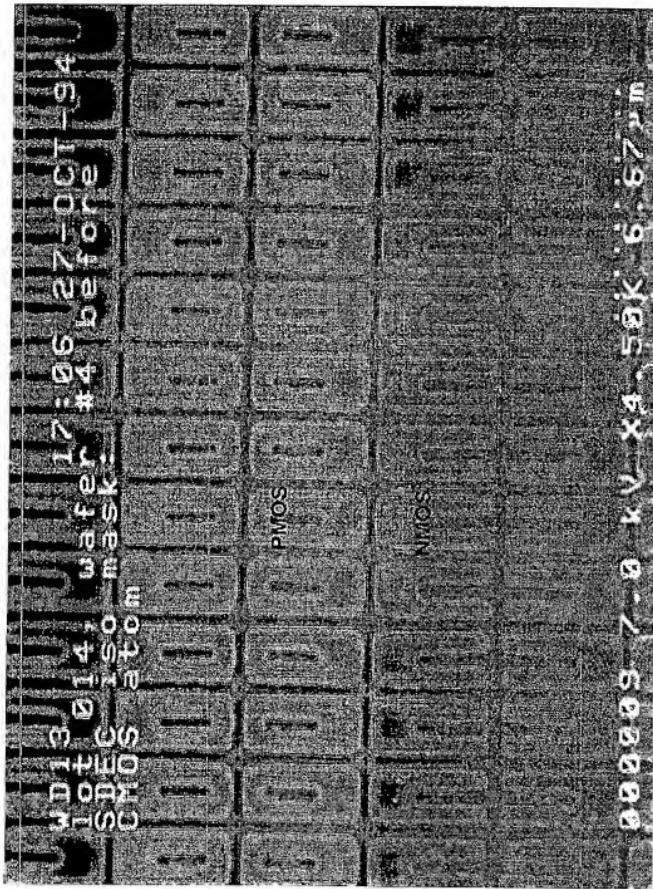


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CMOS Atoms



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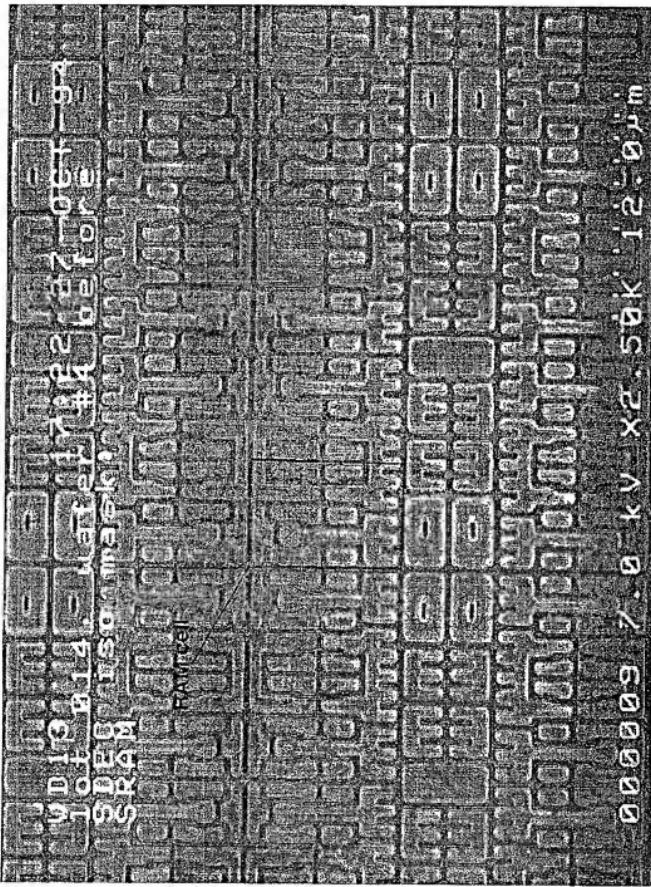
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RAM Cell



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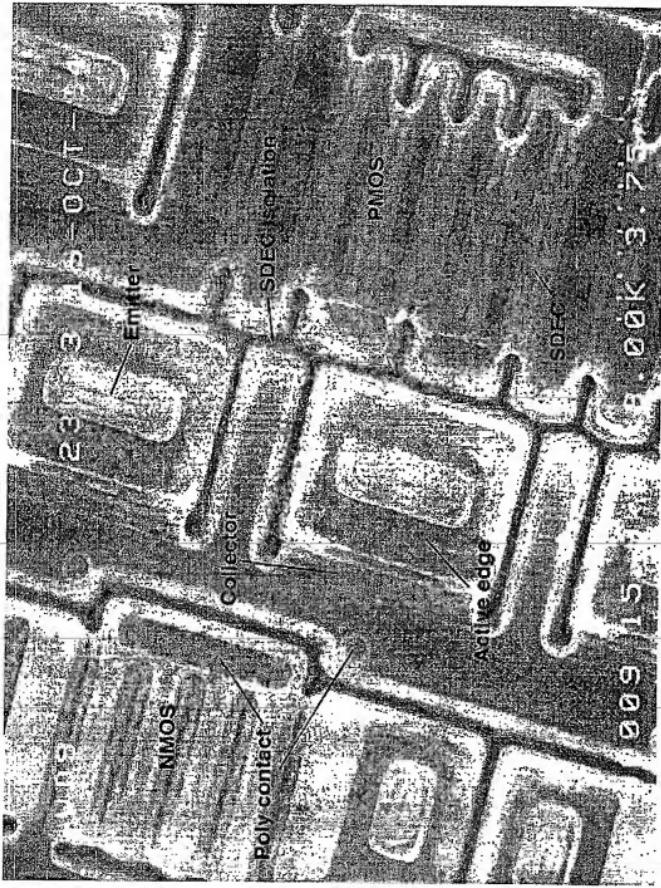
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SDEC, SDEC Isolation and CoSi₂

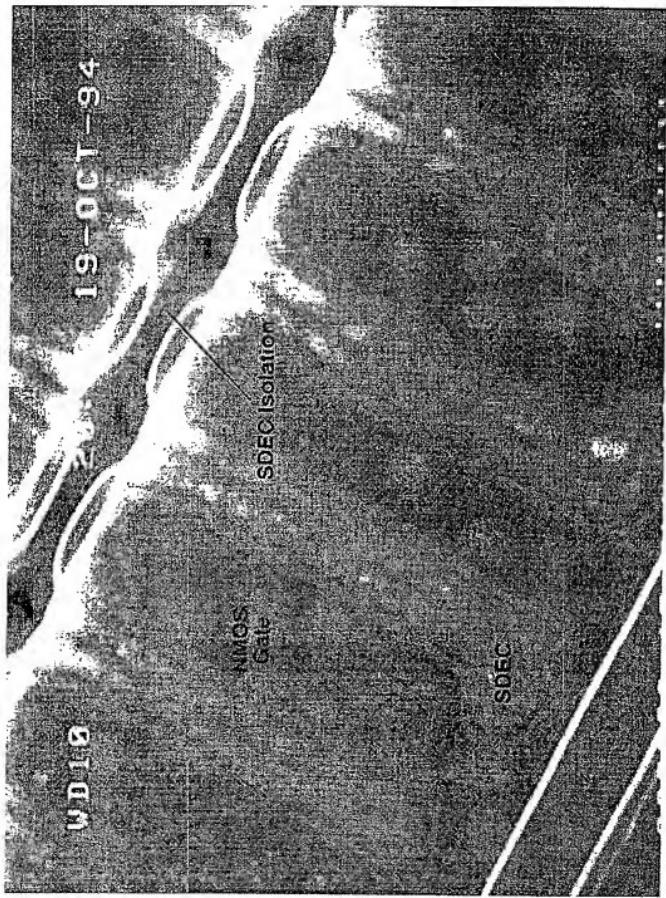


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SDEC Isolation close-up



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Process Status (continued)

■ Metallization

- There are two basic metal systems in use for the process:
Ti/Pt/Au and Nb/Au

The Nb/Au system is usable up to 400C* for extended times (longer than 1 hour).

The Ti/Pt/Au system is being used for the initial barrier between the metal systems and the transistors.

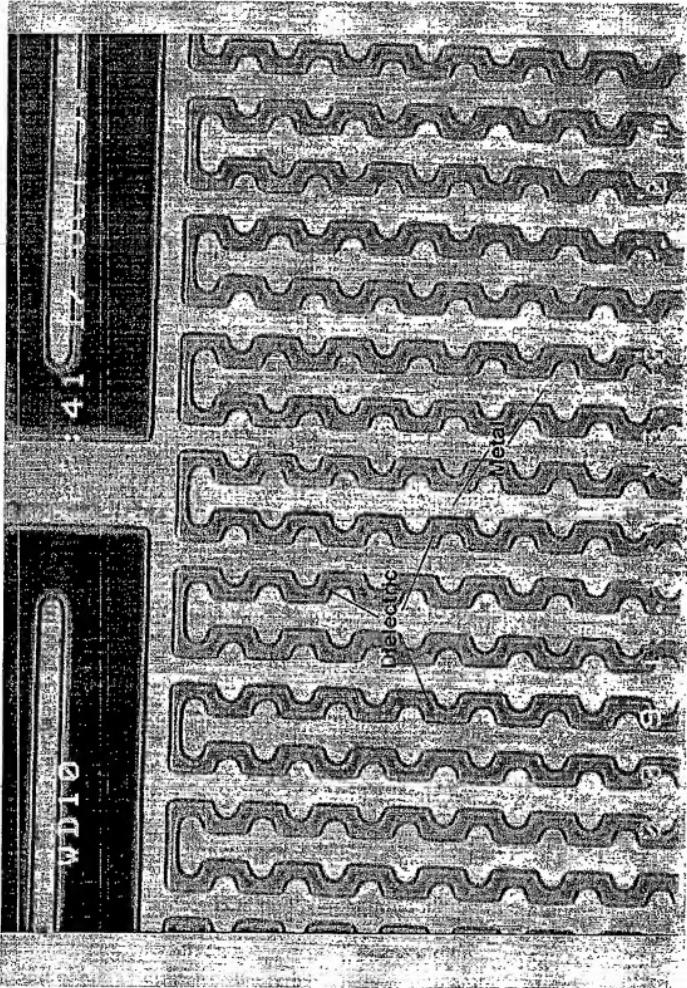
- Lift-off is being used to pattern the metal layers
Lift-off of the Ti/Pt/Au stack has been demonstrated
Tests on the Nb/Au stack are just starting
Multi-layer metal demonstrations (space transformer) are underway.

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Metal Short and Open Test Structure



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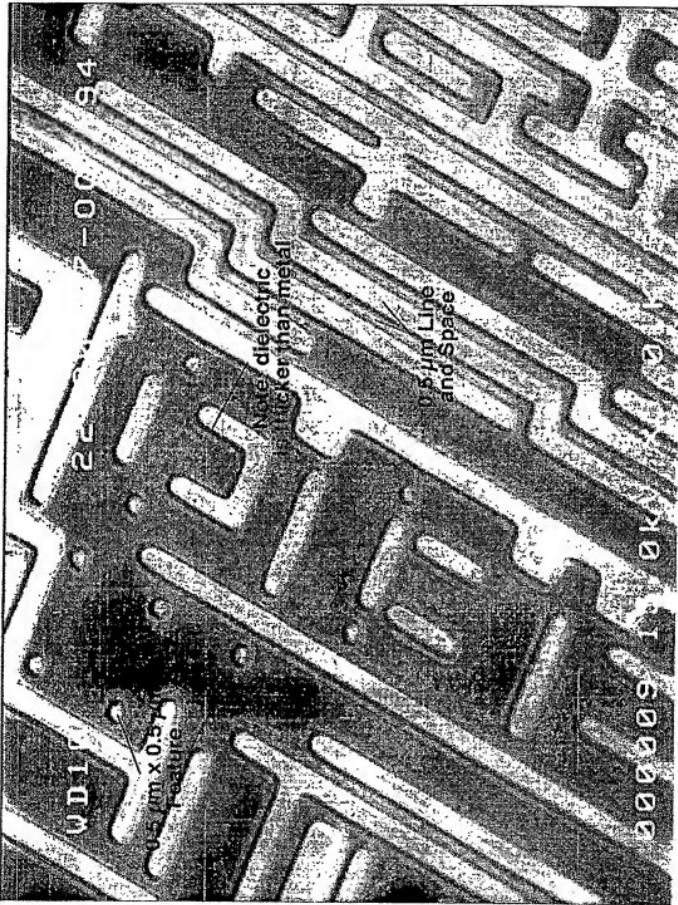
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Metal Lift-off



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Process Status (continued)

■ Packaging

- Flip-chip bonding

Currently only thermal compression is available - probably not suitable for production devices

AuGe eutectic bonding has been tested, equipment modifications are underway and should testing should resume in about a week

Pb and PbIn solder methods are being evaluated
Production equipment still needs to be specified.

- TAB ILB

Initial tests are complete

System is usable but some issues remain.

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Process Status (continued)

■ Packaging (continued)

- Air bridge

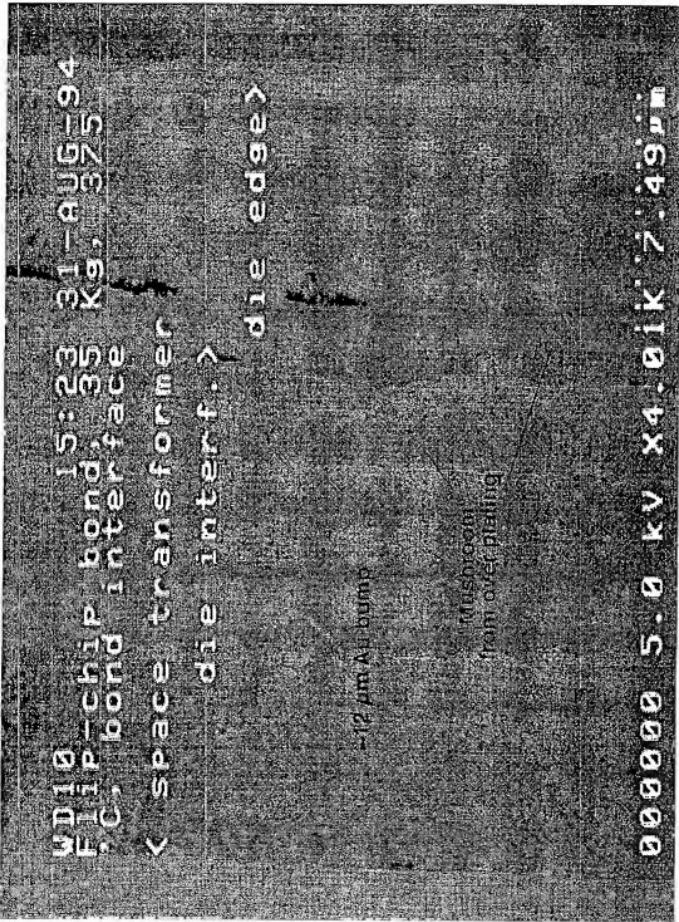
Initial tests will start next week on forming the air bridge.

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Thermocompression Seal Ring



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MicroUnity I.C. Process Status

Current Device Status

■ Castor/Pollux

- Process and circuit test vehicle

As of 10/28 there are 17 lots of this device in the line with the lead lot at CoSi₂ patterning mask.

■ Orchis

- Yield and burn-in test vehicle, 1 Mbit SRAM
11 lots in the line, lead lot at SDEC isolation mask.

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Current Device Status (continued)

- Calliope
 - Product I/O device
 - 11 lots in the line, lead lot at CoSi₂ patterning mask.
- Euterpe
 - Product MPU
 - This product is currently in final baseplate verification, we expect reticles for it by mid to late November.

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MicroUnity I.C. Process Status

Documentation

■ Design Rules

- Currently in revision 4.4, 163 pages.
- Next revision, 5.0, is due out after initial lots are completed through the line.

■ SPICE Model

- Current model based on process (SUPREM-4) and device (PISCES-2B) simulations and device characterization from earlier foundry devices.
- Models are at the BSIM-2 level.

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Documentation (continued)

■ Process Specifications

- All process specifications are on-line in the CIM system
- The specifications are being written as the process step are stabilized, currently most process steps are running without formal specifications.

■ CIM System

- The system is being written in house, it is a graphically based data base system.
- Lots are currently tracked and operations verified on the system, lot and equipment comments are being recorded.
- Video input and equipment status logs are planned.

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MicroUnity I.C. Process Status

Summary

- All process equipment is in and running
- Transistors to E-test are expected within about two weeks
- First lots are expected out by the end of November
- First yield should occur within three weeks of the completion of the first lots
- First packaged parts (for physical tests) should be complete by the end of November

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Summary (continued)

- Process issues to be addressed at this time include:

- Spacer etch time optimization.
- SDEC etch back time optimization.
- Implant adjustment to meet device specifications.
- Metal lift-off profile control interactions with dielectric stack.
- Flip-chip bond method evaluation.
- TAB ILB equipment issues (auto align and TAB finger placement).
- Air bridge process bring up.

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Characteristics

- Byte addressing, 64-bit virtual address space
 - 8-, 16-, 32-, 64-, 128-bit memory transfers
- 64-bit general registers
- 32-bit, aligned instructions
- Simplest possible user state
- High-bandwidth memory
- Precise exceptions

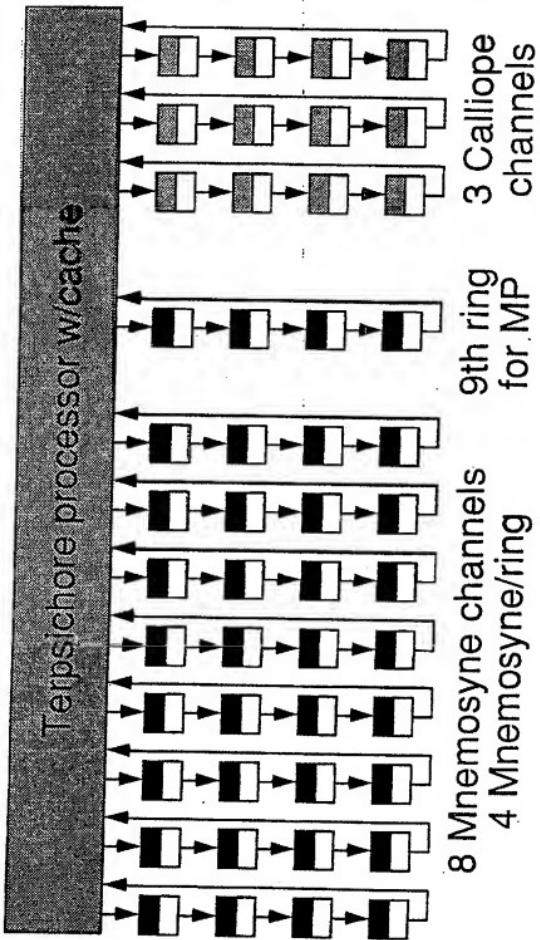
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Terpsichore memory structure



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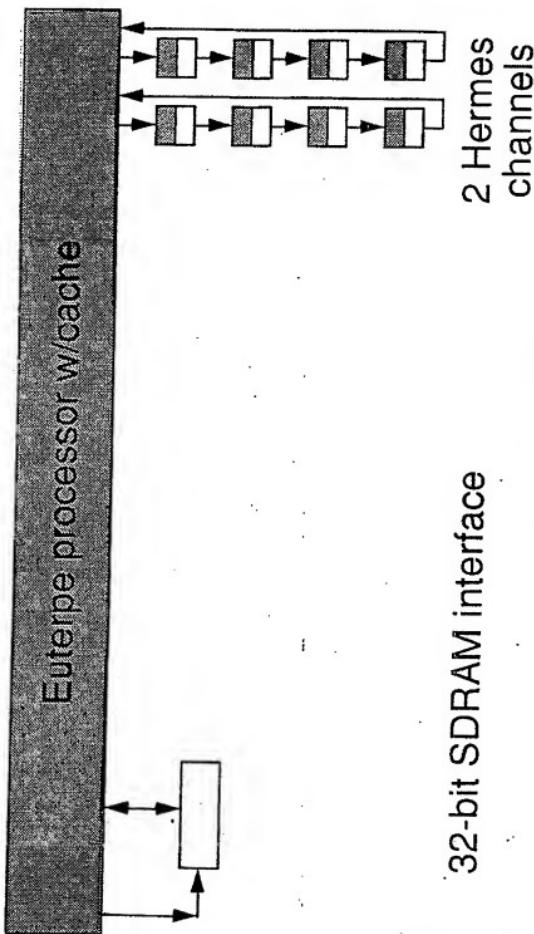
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Euterpe memory structure



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Euterpe subset implementation

- no floating-point
- no interprocessor communications
- no strong/sequential memory ordering
- no unaligned memory access
- 2 Hermes channels, subset of full Hermes interleaving patterns: no octlet and no multiprocessor interleaves
- no EGFMUL64, G{\, U}DIV,
G{\{, U\}}MUL{\, ADD},ADD,SUB,SET},\{2,4\}

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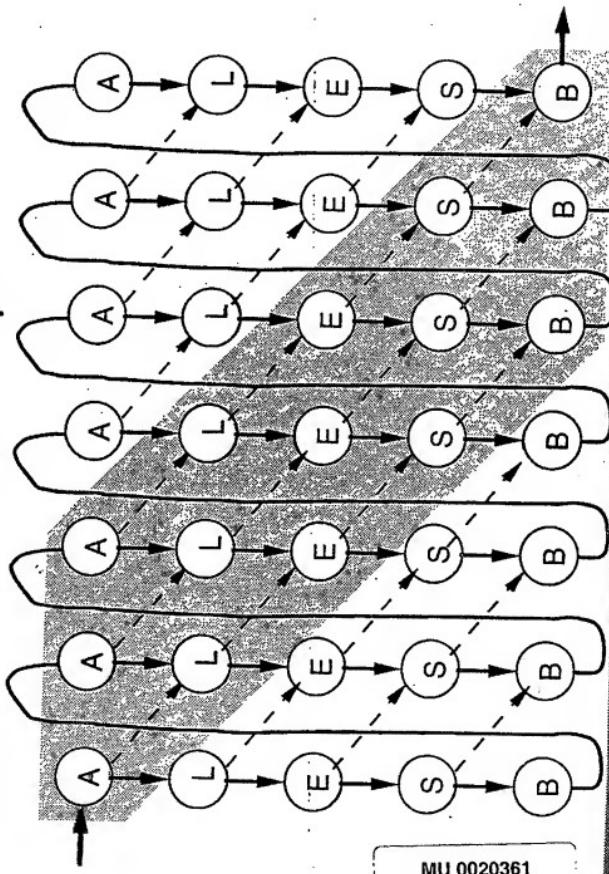
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Superscalar Pipeline



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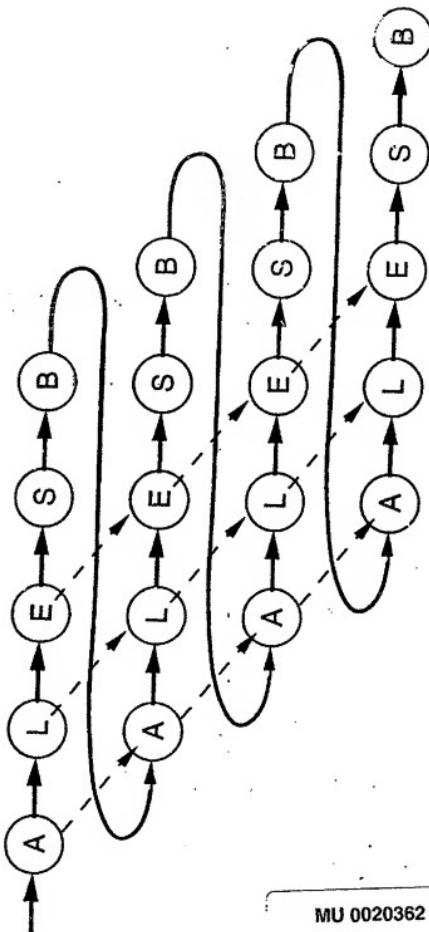
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Superstring Pipeline



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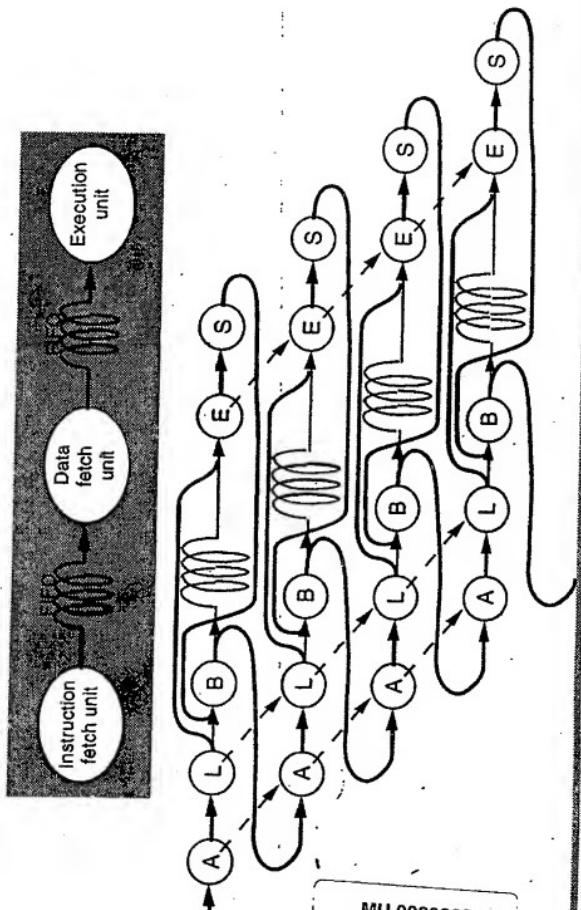
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Superspring Pipeline



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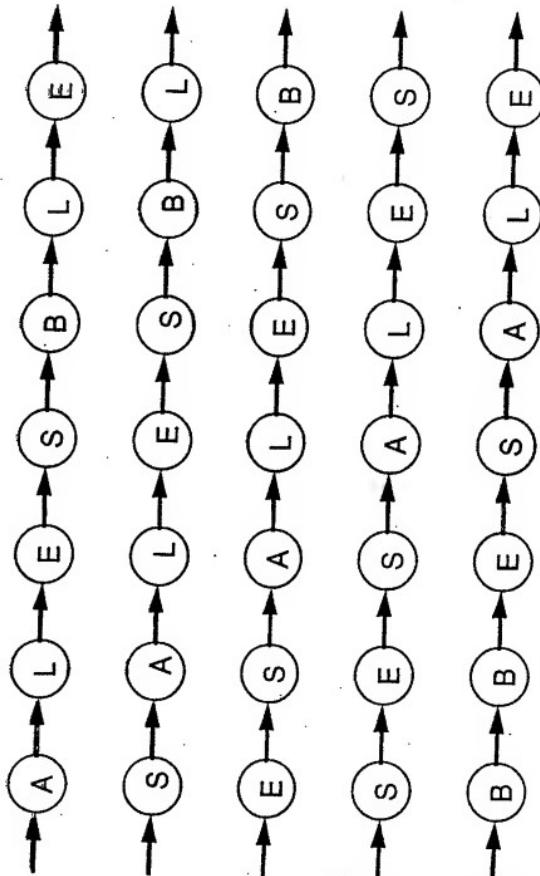
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SuperThread Pipeline



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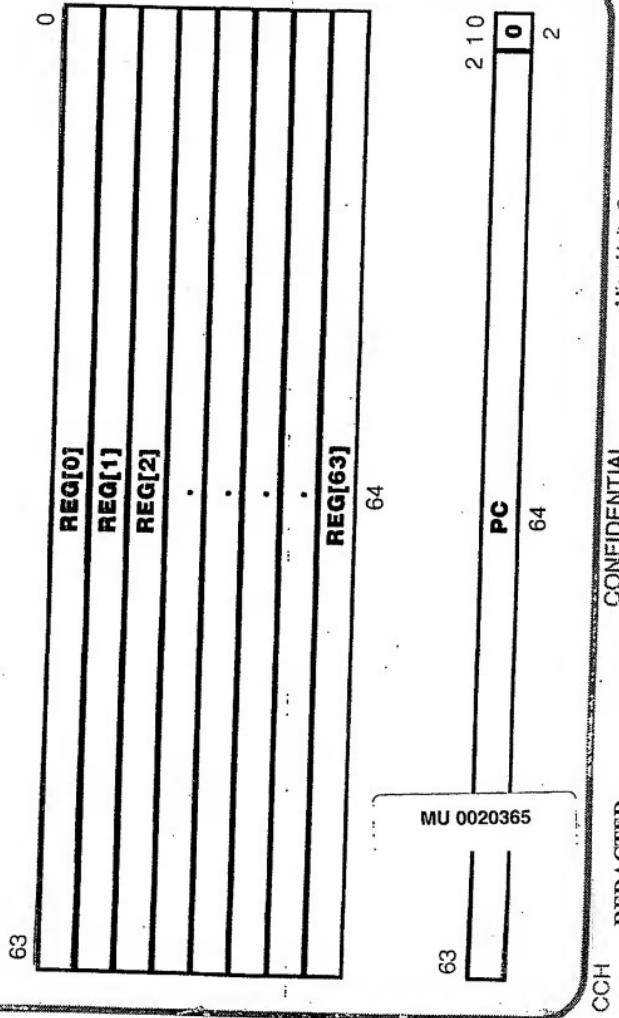
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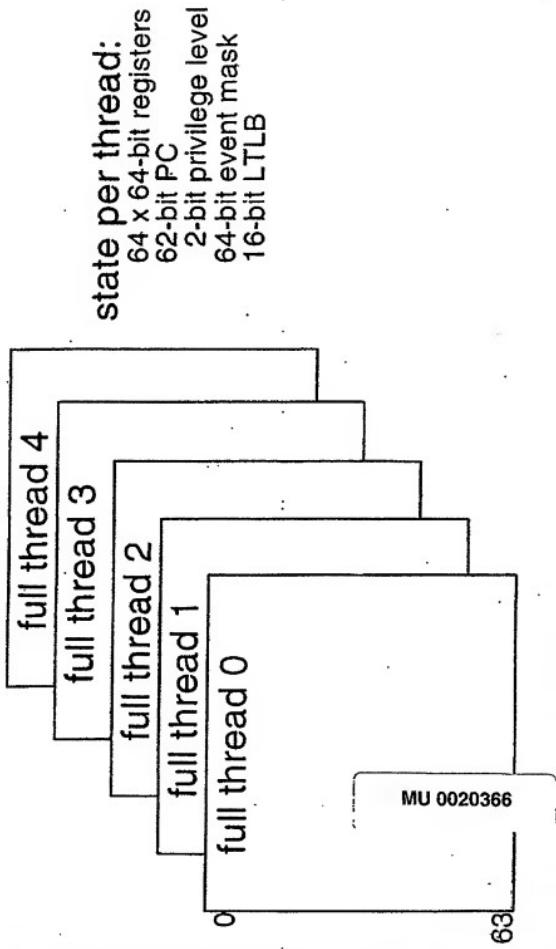
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User state



SuperThread state



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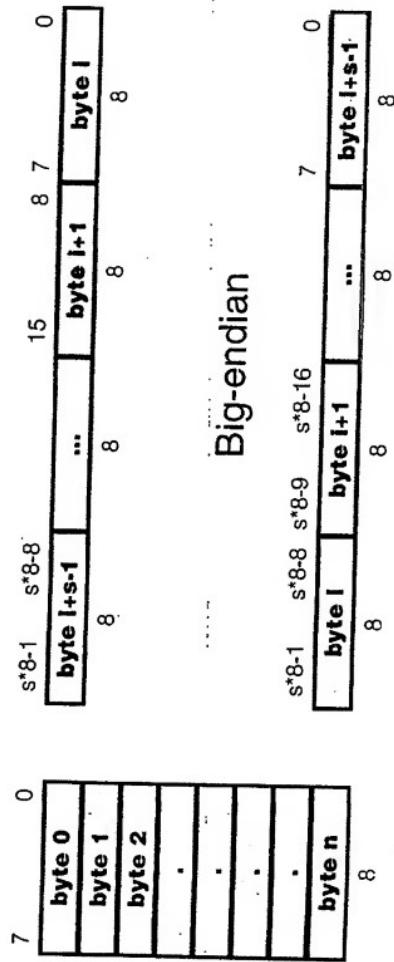
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Data Representation

Memory



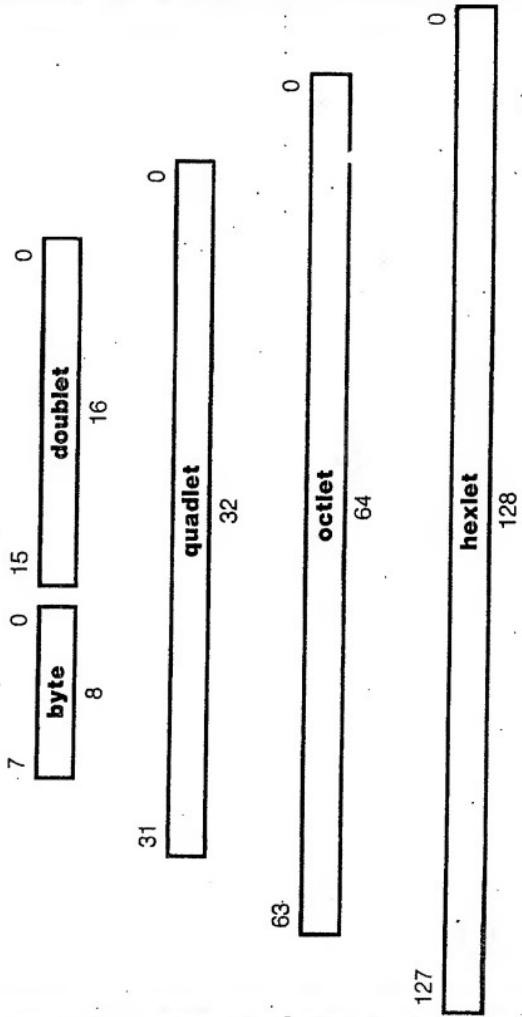
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Fixed-Point Data Sizes



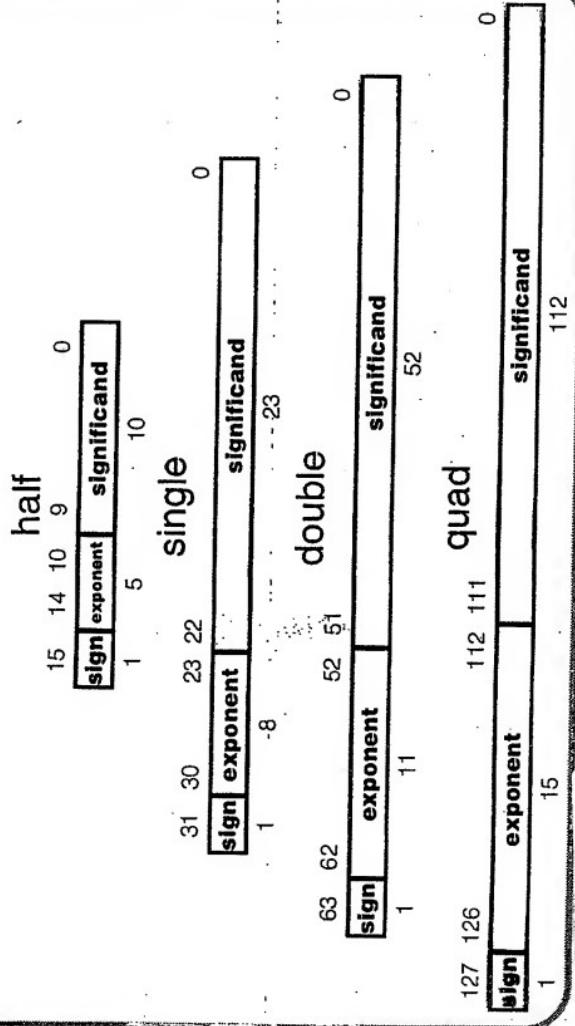
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Floating-point Data Sizes



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Instruction Formats

31	24	23	0
8	major	ra	imm
31	24	23	0
8	major	ra	rb
31	24	23	0
8	major	ra	rb
31	24	23	0
8	major	ra	rc
31	24	23	0
8	major	ra	rd

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Major Operation Codes

MAJOR	0	32	64	96	128	160	192	224
0	EYES	GSHUFFLEI	GMULADD16	LU16AI	SAAS64AI	EADDIO	BFE16	
1	ESHUFFLEMUX	GSHUFFLEMUX	GMULADD32	LU16BAI	SCAS64BAI	EADILIO	BFRNGE16	
2	EMDEPI	GSELECT8	GMULADD64	LU16LI	SCAS64LAI	ESETIL	BFRNGL16	
3	EMUX	GNDEPI	FMULSUB16	GMULADD16	LU32AI	SCAS64AI	BFE32	
4	EBMULX	GNLUX	FMULSUB32	GMULADD32	LU32BAI	SCAS64BAI	BENJU32	
5	EGFMUL64	GGFMUL8	FMULSUB64	GMULADD64	LU32LI	SMJX64AI	BENJU32	
6	ETRANSPOSE&MUL	GTRANSPOSE&MUL	GEXTRACT128	LU32BI	SJX64BAI	ESETIJU	BPNJU32	
7	ESWIZZLE	GSWIZZLE	GUNLUADD2	L16AI	S16AI	ESUBIO	BFE64	
8	ESWIZZLE	GSWIZZLE COPY	GUNLUADD4	L16AI	S16BAI	ESUBIO	BFNUGE64	
9	ESWIZZLE	GSWIZZLE SWAP	GUMLUADD8	L16LI	S16LI	ESUBIL	BFNUGL64	
10	EDEPI	GUDEPI	GUMLUADD16	L16BI	S16BI	ESUBGE	BENJU64	
11	EUDEPI	GUWTHI	GUMLUADD32	L32AI	S32AI	ESUBIE	BENJU64	
12	EDEP1	GUWTHI	GUMLUADD64	L32BAI	S32BAI	ESUBIE	BENJU28	
13	EUWTHI	EUWTHI	GUETRACT128	L32LI	S32LI	ESUBIL	BFRNGE128	
14	EWTHI	EWTHI	GUETRACT16	L32BI	S32BI	ESUBGE	BFRNGL128	
15	EWTHI	EWTHI	GEXTRACT16	L64AI	S64AI	EADDI	BANDIE	
16			GEXTRACT32	L64AI	S64AI	EXORI	BBLZ	
17			GEXTRACT64	L64LI	S64LI	EORI	BGE/BGEZ	
18			GEXTRACT96	L64BI	S64BI	EANDI	BE	
19			GEXTRACT128	L128AI	S128AI	ESUBI	BFE	
20			GEXTRACT16	L128BI	S128BI	ENORI	BUL/GZ	
21			GEXTRACT32	L128LI	S128LI	ENANDI	BULE/BLZ	
22			GEXTRACT64	L128BI	S128BI	SGATEI		
23			GFMULSUB128	G.1	LBI			
24			GFMULSUB16	G.2	LUBI			
25			GFMULSUB32	G.4				
26			GFMULSUB64	G.8				
27			GFMULSUB128	G.16				
28			GFMULSUB16	G.32				
29			GFMULSUB32	G.64				
30			GFMULSUB64	G.128				
31			GFMULSUB128					

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Minor Operation Codes: F, GF

F.size	0	8	16	24	32	40	48	56
0	FADD.N	FADD.T	FADD.F	FADD.C	FADD.X	FSETE.X	FSETNUEX	FSETNUEX
1	FSUB.N	FSUB.T	FSUB.F	FSUB.C	FSUB.X	FSUB.X	FSETNUEX	FSETNUEX
2	FMUL.N	FMUL.T	FMUL.F	FMUL.C	FMUL.X	FMUL.X	FSETNUEX	FSETNUEX
3	FDIV.N	FDIV.T	FDIV.F	FDIV.C	FDIV.X	FDIV.X	FSETNUEX	FSETNUEX
4	F.UNARY.N	F.UNARY.T	F.UNARY.F	F.UNARY.C	F.UNARY.X	F.UNARY.X		
5								
6								
7								

GF.size	0	8	16	24	32	40	48	56
0	GFADD.N	GFADD.T	GFADD.F	GFADD.C	GFADD.X	GFADD.X	GFSETE.X	GFSETE.X
1	GFSUB.N	GFSUB.T	GFSUB.F	GFSUB.C	GFSUB.X	GFSUB.X	GFSENUEX	GFSENUEX
2	GFMLN.N	GFMLN.T	GFMLN.F	GFMLN.C	GFMLN.X	GFMLN.X	GFSETNUEX	GFSETNUEX
3	GFDIV.N	GFDIV.T	GFDIV.F	GFDIV.C	GFDIV.X	GFDIV.X	GFSETNUEX	GFSETNUEX
4	GF.UNARY.N	GF.UNARY.T	GF.UNARY.F	GF.UNARY.C	GF.UNARY.X	GF.UNARY.X		
5								
6								
7								

F.UNARY.size	0	1	2	3	4	5	6	7
0	F.ABS	GF.ABS						
1	F.NEG	GF.NEG						
2	F.SQR	GF.SQR						
3								
4	F.SINK	GF.SINK						
5	F.FLOAT	GF.FLOAT						
6	F.INFLATE	GF.INFLATE						
7	F.DEFLATE	GF.DEFLATE						

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Minor Operation Codes: E, G

E/MINOP	0	8	16	24	32	40	48	56
0	EADD	ESUBO	EANDN	EADD	ESUB	ESHLO	ESHLO	ESHRI
1	EADDO	ESUBO	EXOR	ESHLO	ESUB	ESHLUO	ESHLUO	EUSHRI
2	ESETL	ESUBOE	EAND	ELMS	EASUM	ESELECTB	ESHUFFLEI	EROTRI
3	ESETGE	ESUBOE	EOR	EASUM	EROTL	ESHRL	ESHLI	ENSHRI
4	ESETE	ESUBNE	EORN	EROTR	ESHRL	EMSHR		
5	ESETNE	ESUBNL	EANOR					
6	ESETUL	ESUBNL	ENOR					
7	ESETUGE	ESUBGE	ENAND					

G/size	0	8	16	24	32	40	48	56
0	GADD	GMUL	GANDN	GADD	GSUB	GUCOMPRESS	GEXPAND	GSHR
1	GSETL	GUML	GOR	GCMPRESS	GUEXPAND	GUEXPAND	GUEXPAND	GUHR
2	GSETGE	GDIV	GAND	GCMPRESS	GUEXPAND	GUEXPAND	GUEXPAND	GHOTR
3	GSETNE	GSUB	GORN	GCMPRESS	GUHR	GUHR	GUHR	GMHRI
4	GSETUL		GXROR	GCMPRESS	GRTR	GRTR	GRTR	
5	GSETUGE		GRAND					
6								
7								

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Minor Operation Codes: L, S, B

L/min	0	8	16	24	32	40	48	56
0	L16LA	L16LA	L64A	L8				
1	L16BA	L16BA	L64BA	L8B				
2	L16L	L16L	L64L					
3	L16B	L16B	L64B					
4	L32LA	L32LA	L128LA					
5	L32BA	L32BA	L128BA					
6	L32L	L32L	L128L					
7	L32B	L32B	L128B					

S/min	0	8	16	24	32	40	48	56
0	SAAS64LA	S16LA	S64LA					
1	SAAS64BA	S16BA	S64BA					
2	SCAS64LA	S16L	S64L					
3	SCAS64BA	S16B	S64B					
4	SMAS64LA	S32LA	S128LA					
5	SMAS64BA	S32BA	S128BA					
6	SMUX64LA	S32L	S128L					
7	SMUX64BA	S32B	S128B					

B MINOR	0	8	16	24	32	40	48	56
0	8LINK							
1	BLINK							
2	B DOWN							
3								
4								
5								
6								
7								

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Branches

- Non-delayed branches
- Fixed-point compare and branch
 - equal, not equal, less, or greater/equal
 - two-operand signed or unsigned compare
 - bitwise and, then compare vs. zero
- Floating-point compare and branch
 - Classic comparisons
 - IEEE-aware comparisons
 - half, single, double, or quad precision
- Unconditional branch
 - pc+offset or register
 - save link (register 0)

Floating-point Compare

Mnemonic	Branch taken if values compare as:				Exception if unordered
code	C	Unordered	Greater	Less	Equal
E	==	F	F	F	T
NUGE	?>=	F	F	T	F
NUL	?<	F	T	F	T
UL	?<	T	F	T	F
UGE	?>=	T	T	F	T
NE	!=	T	T	T	F
LNGE	<,!>=	F	T	F	yes
GE,NL	<=,!>	T	F	T	yes

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Privilege-level crossing branches

- Four privilege levels held in least-significant peck of PC
- Branch gateway
 - secure equivalent to L128L1+B+increase in privilege
- Branch down
 - secure equivalent to B+decrease in privilege
- Branch back
 - secure equivalent to L128L1+B+decrease in privilege
 - permits complete restoration of register state after event

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Loads, Stores

- Byte addressing
- Big-endian or little-endian
- Byte, doublet, quadlet, octlet, hexlet
- Signed or unsigned (byte, doublet, quadlet)
- Aligned or unaligned (doublet, quadlet, octlet, hexlet)
- Base register + 12-bit signed offset
- Base register + index register
- Large immediates are loaded, not constructed

Synchronization

- Sequentially consistent and weak ordering
 - Specified in TLB entry
 - Synchronization operations always sequentially consistent
- Aligned octlet operations
 - Swap (load mem->reg, store reg->mem)
 - Add (load mem->reg, add reg+mem->mem)
 - Compare&Swap (load mem->reg, compare reg<->reg, if equal, store reg->mem)
 - Masked-write (load mem->reg, mux:mask, reg,mem->mem)

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Fixed-point

- Shifts, add, subtracts
- Explicit overflow checking
- Bitwise logical operations
- Compare and set boolean
- Register or 12-bit signed immediate
- Integer multiply and divide

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Floating-point

- Half, single, double, quad precision
- Add, sub, mul, div, sqr, abs, neg
- Combined multiply, add/subtract
- Format conversions
- Explicit rounding selection
- Explicit exception handling
- Explicit inexact checking

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Special-Purpose Instructions

- Find most significant one
- Count ones
- Bitwise multiplex
- Deal & Shuffle
- Gather & Scatter
- Galois Field Multiply

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Find most/least significant one

E.ULMS rc,ra

```
t ← REG[ra]
if t = 0
    res ← -1
else
    res ← i :: (ti = 1 and t63..i+1 = 0)
endif
REG[rc] ← res
```

Most-significant:

E.ULMS rt,rs

Least-significant:

E.ADDI	rt,rs,-1
E.ANDN	rt,rt,rs
E.ULMS	rt,rt

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Count Ones

E.ASUM rc,ra,rb

```
t ← REG[ra] & REG[rb]
res ← 0
for i ← 0..63
    res ← res + t
endfor
REG[rc] ← res
```

Count Ones:

E.ASUM rt,rs,rs

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Multiplex

E.MUX rd,ra,rb,rc

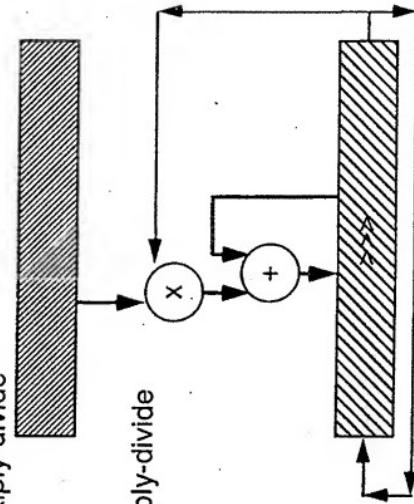
$t \leftarrow \text{REG}[ra]$
 $\text{REG}[rd] \leftarrow (t \& \text{REG}[rb]) \mid (\sim t \& \text{REG}[rc])$

G.MUX rd,ra,rb,rc

$t \leftarrow \text{REG}[ra] \parallel \text{REG}[ra+1]$
 $\text{REG}[rd] \parallel \text{REG}[rd+1] \leftarrow \begin{cases} (t \& (\text{REG}[rb] \parallel \text{REG}[rb+1])) \\ (\sim t \& (\text{REG}[rc] \parallel \text{REG}[rc+1])) \end{cases}$

Galois Field Arithmetic

- E.GFMUL.64
 $GF(2^{64})$ multiply
64-bit polynomial multiply-divide
- G.GFMUL.8
 $GF(2^8)$ multiply
8-bit polynomial multiply-divide

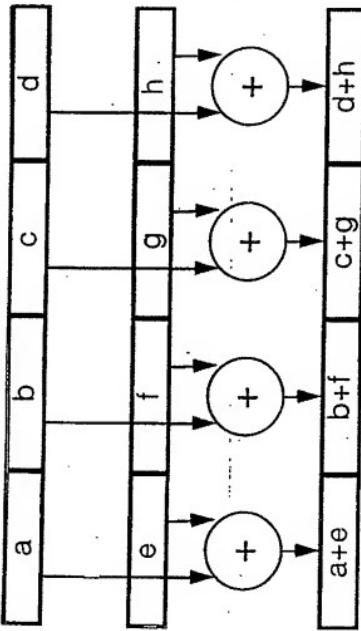


Group (DSP) Operations

- Designed to be accessible to compilers
- Operate on 128 bit vectors
- Fixed-point data sizes 1, 2, 4, 8, 16, 32, 64 bits
- Floating-point data sizes 16, 32, 64 bits
- Multiply, add/subtract, shift/rotate
- Combined multiply, add/subtract
- Flexible size and format conversion

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Group Add



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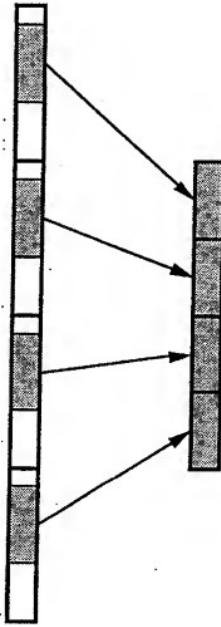
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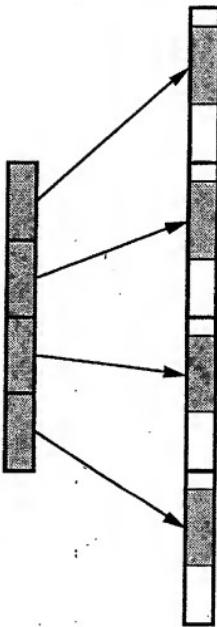
Group Compress, Extract

- Group Compress: 128 bits to 64 bits
 - immediate and dynamic shift amounts for all sizes: 1-64 bits
- Group Extract: 256 bits to 128 bits
 - immediate shift amounts for all sizes: 1-128 bits
 - dynamic shift amounts for 128 bits



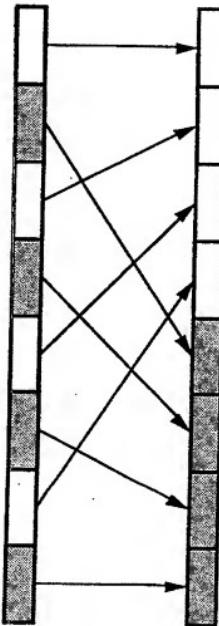
Group Expand

- Group Expand: 64 bits to 128 bits
 - immediate and dynamic shift amounts for all sizes: 1-64 bits
 - signed and unsigned expand

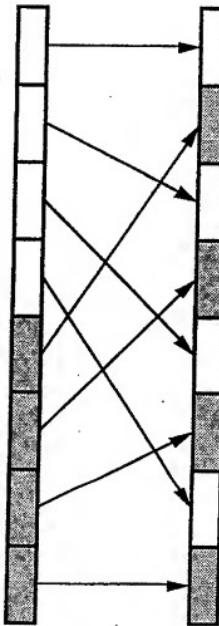


Group Deal, Shuffle

- Group Deal: 128 bits to 128 bits



- Group Shuffle: 128 bits to 128 bits



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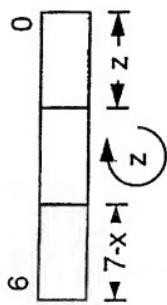
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Group Shuffle

- General form: GSHUFFLE $1.2^x.2^y.2^z$



$$\text{imm} = (x \cdot 3x^2 \cdot 4x)/6 - (z^2 \cdot z)/2 + xz + y + 1$$

Group Shift

- Group Shift: 128 bits
 - shift or rotate at 2, 4, 8, 16, 32, 64, 128 bit granularity
 - dynamic: ROTL, ROTR, SHL, SHR, USHR, MSHR
 - immediate: ROTRI, SHLI, SHRI, USHRI, MSHRI
- Group Deposit/Withdraw: 128 bits
 - deposit or withdraw at 2, 4, 8, 16, 32, 64, 128 bit granularity
 - field_size from 1..size, shift_amount from 0..field_size
 - immediate field_size and shift_amount only

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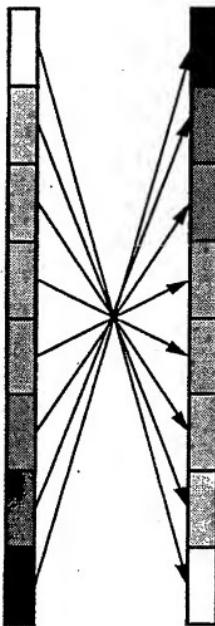
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Group Swizzle (Copy-Swap)

- Group Swizzle (Copy-Swap): 128 bits
 - copy and/or swap at 1, 2, 4, 8, 16, 32, 64 bit granularity



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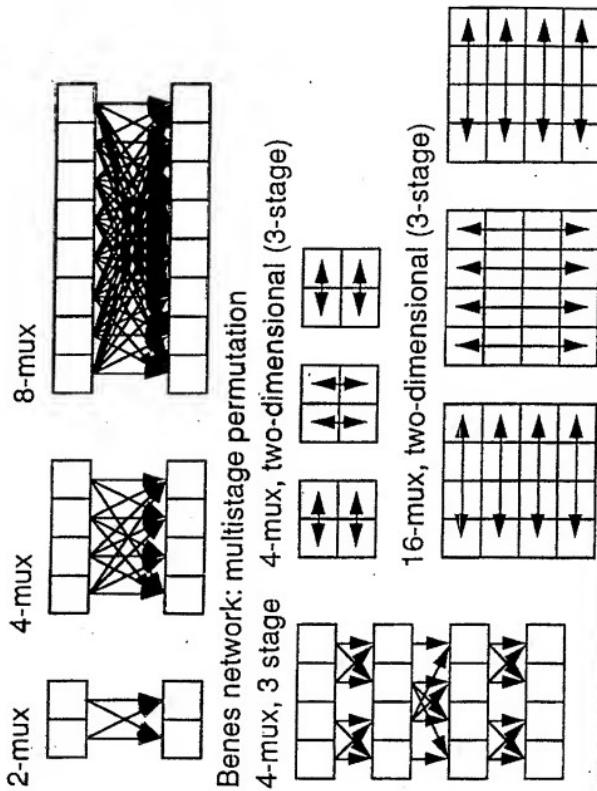
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Group Permute



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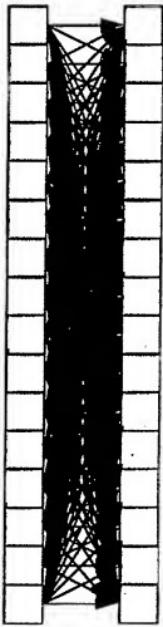
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Group Permute

- two dimensional network
 - 8-mux, 16-mux, 8-mux
 - same network used for shifts, rotates, shuffles, permute
 - network itself capable of arbitrary permute, but instructions can't provide sufficient control bits in a single instruction
- G.SELECT.8

128 bits data, 4x16=64 bits control

16-way mux, byte-level granularity: complete byte permute
16-mux



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Group Permute

- **G.SHUFFLE1.4MUX**
 - 128 bits data, 2x64 bits control
 - 4-way mux with shuffle
 - 3 passes perform complete 16-bit permute
 - 5 passes perform complete 64-bit permute
- **G.8MUX, G.TRANSPOSE.8MUX**
 - 128 bits data, 3x64 bits control
 - 8-way mux with optional transpose (triple shuffle)
 - 3 passes perform complete 64-bit permute

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System Facilities

- All system state memory-mapped
- All system code can be compiled
- Lightweight exception and event handling
- Protected gateways
- Virtual-addressed, virtual/physical-tagged internal caches
- Internal buffer memory
 - Cache tags
 - Interprocessor communication buffers
 - I/O transfer buffers

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Virtual Memory

- Arbitrary virtual to physical maps
 - any page size
 - frame buffer, physical kernel spaces use one TLB entry each
 - allocation of physically interleaved memory to virtual space
- 64-bit virtual addresses
- Virtual caches with support for aliases
 - up to 4 privilege levels, in TLB
 - up to 16 bit address space identifiers
 - asid part of virtual address

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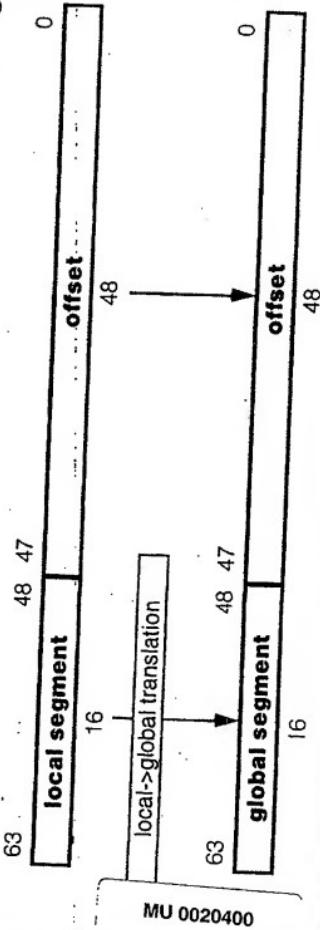
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Need VM space be > 64 bits?

- 64 bit space is more than large enough
- Segmentation vs matching
- UNIX fork requires process-local addressing
- kernel and library code prefers global addressing



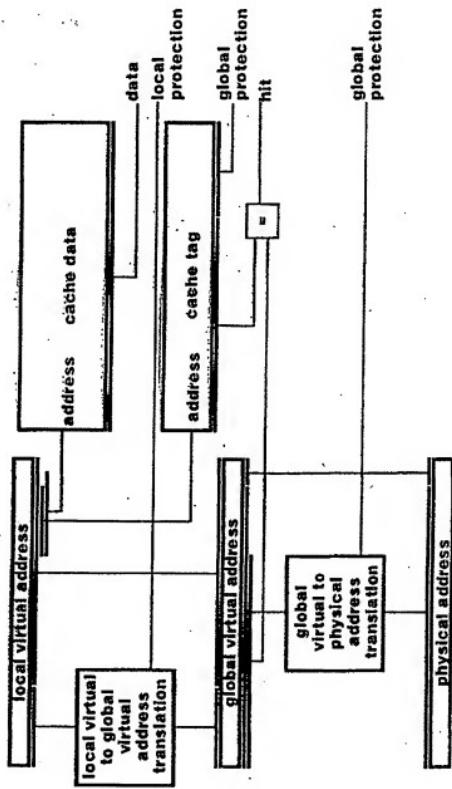
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Translation Block Diagram



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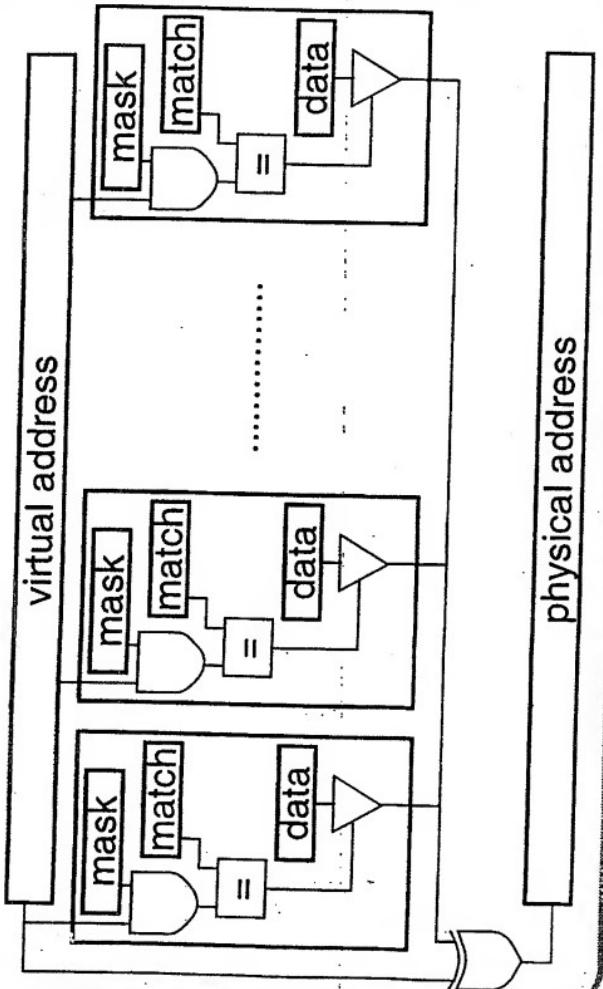
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Translation Lookaside Buffer



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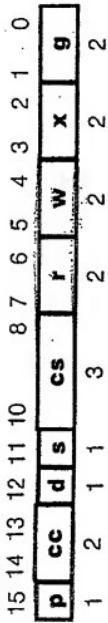
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Protection information



- r,w,x,g: minimum privilege for access
- cc: cache control
 - 0: cached, 1: coherent, 2: noallocate 3:physical
- cs: coherence state
 - 4: read, 2: write, 1: replace
- p: priority, d: detail, s: sequential

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Exceptions and Events

- Exceptions post events
- Events handled via minimal context switch
 - program counter and general register saved in D memory
 - Multiple events remain queued in event register
 - program counter & general register loaded from D memory
- Memory-mapped resources
 - Event register
 - Suspended thread's program counter & general register
- Precise exceptions, never masked

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I/O structure

- Data moved by loads & stores (no DMA)
- Movement via event thread
- External interface chips - "Calliope"
 - buffer memory
 - buffer processor
 - timing generator
 - device formatters
 - device-specific interfaces

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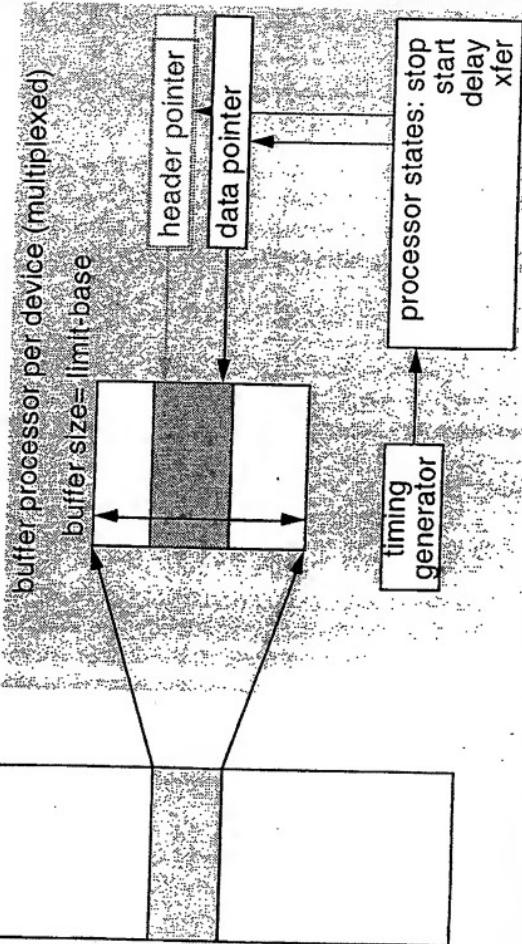
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Calliope buffer memory and processor

Calliope buffer space



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Summary

- Full 64-bit general-purpose architecture
- Gigaflop supercomputer performance
- DSP capable of video and audio
- Powerful and flexible Gigabit I/O system

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Mux operations viewed as functions on bit indices

- An arbitrary mux operation may be viewed as a function on the bit index:

$$\text{dest}[i] \leftarrow \text{src}[f(i)]$$

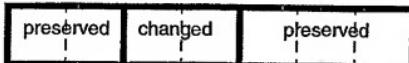
- The number of high index bits preserved by the function determines the “outer” group size.
- The number of low index bits preserved by the function determines the “inner” group size.

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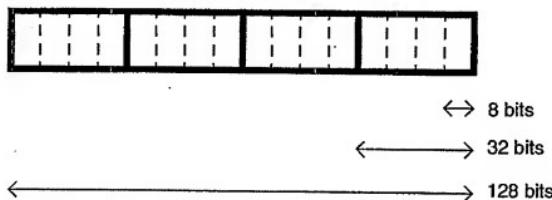
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- For a 128-bit datapath, a bit index is 7 bits wide. If we preserve 2 high-order index bits, then we are operating on 4 groups of 32 bits. If we further preserve 3 low-order index bits, then we are operating on 8-bit groups within each 32-bit group.



This corresponds to an “outer” group size of 32 and an “inner” group size of 8.



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MicroUnity Systems Engineering, Inc. Mux operations viewed as

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- A “copy” operation, on bits, pecks, nibbles, etc., corresponds to setting a consecutive sequence of index bits to constant values.
- A reversal, or “swap”, operation on bits, pecks, nibbles, etc., corresponds to complementing a consecutive sequence of index bits.
- A rotate operation corresponds to performing modular addition on a consecutive sequence of index bits.
 - Zero fill and sign extend can be achieved through minor modifications of this.
 - Expand and compress operations can be achieved by additionally performing right or left shifts on the high-order index bits.

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MicroUnity Systems Engineering, Inc. Mux operations viewed as

- A shuffle/deal operation corresponds to performing a rotation on a consecutive sequence of index bits.
 - Viewed as any power-of-two rectangular matrix, a transpose of that matrix corresponds to a perfect shuffle/deal of some order.
 - Viewed as any power-of-two n-dimensional rectangle, an arbitrary transposition of the dimensions corresponds to a permutation on a consecutive sequence of index bits. Although it is possible to implement this generality, the encoding is somewhat cumbersome and requires too many bits to fit in an immediate.
- All of these functions on bit indices seem fairly easy to compute. However, a full crossbar for performing the data muxing is expensive to build. Is there a cheaper way?

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General permutation algorithms

- It can be shown that an arbitrary permutation of W bits can be performed by first arranging the data in an n-dimensional rectangle whose sides correspond to the factors of W. The permutation can then be achieved by performing a sequence of independent permutations along each dimension, followed by a second sequence of independent permutations which follows the dimensions in the opposite order, i.e., d₁, d₂, ..., d_n, d_{n-1}, ... d₁. This is a sequence of $2^n - 1$ permutations.

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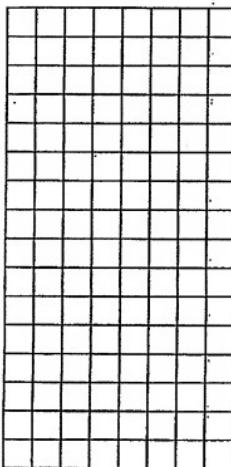
- The case we're interested in is the 2-dimensional case. When arranged as a rectangle, an arbitrary permutation can be achieved by performing the following sequence of operations:
 - a. Perform a set of independent row permutations on the data.
 - b. Perform a set of independent column permutations on the data.
 - c. Perform a set of independent row permutations on the data.
- If the row and column permutation operations are replaced with mux operations, some copying may also be achieved (although not all cases can be handled).

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The XLU datapath

- Since our machine datapath is 128 bits wide, we are building a permutation network based on a 16 x 8 rectangle:



16 rows

8 columns

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- Data enters along the rows. Each row has 8 data buses.
- Stage 1 consists of performing an 8:1 mux operation on each bit from the 8 data buses in its row. The results are placed on a set of data buses which run along the columns, with 16 buses per column.
- Stage 2 consists of performing a 16:1 mux operation on each bit from the 16 data buses in its column. The results are placed on a set of data buses which run along the the rows, with 8 buses per row,
- Stage 3 consists of performing an 8:1 mux operation on each bit from the 8 data buses in its row. Data leaves along the rows.

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XLU datapath control

- Since each bit has two 8:1 and one 16:1 mux operations performed on it, we would need $128 * (2*3 + 4)$ encoded mux selects to perform all of these operations in the obvious way. This is 1280 independent mux controls. This seems like too much control logic and wiring.
- We can improve on this by generating multiple sets of control signals which are shared along columns (stages 1 & 3) or rows (stage 2), and a set of control selects which is shared along rows (stages 1 & 3) or columns (stage 2).

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- The control for each bit is generated locally by performing an independent mux operation on each of the control bits being shared by that row or column.

For example, for a given bit in stage 1, there are two 3-bit shared control buses in its column, and a 3-bit shared control select bus in its row. Each of the 3 control select bits selects one of the two corresponding control bits. The resulting 3-bit value is then decoded and used to control the 8:1 mux for that bit.

- This breakdown of the XLU control into shared row and column signals significantly reduces the amount of control logic and wiring for the XLU.

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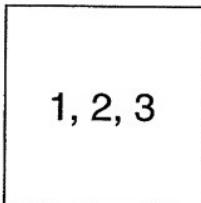
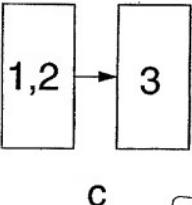
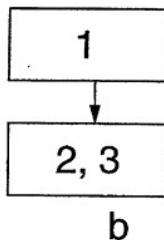
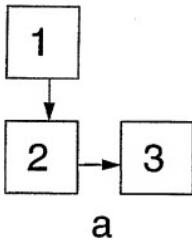
XLU placement and routing

- It is initially intuitive to think of the stage 1, 2, and 3 muxes for a given bit being in close physical proximity to one another. However, this is not necessary. The data flow from stage 1 to stage 2 is along columns, so the stage 1 and stage 2 muxes for a given bit must be in the same column. The data flow from stage 2 to stage 3 is along rows, so the stage 2 and stage 3 muxes for a given bit must be in the same row. This still leaves room for four basic placement strategies.

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- Both a and b have the undesirable property that the data coming in and out isn't aligned with the rest of the datapath.
- Placement c has the advantage that some of the row wires don't need to coexist as they would in d. This is the placement we are using.



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XLU functional control

- The shared row and column control signals for the XLU are generated by several independent control modules, each of which is specific to a particular class of operations. For example, shuffle control, shift/rotate control, copy/swap control, etc.
- These control signals are then selected by a mux operation. The outputs of these mux operations are the shared row and column control signals used for the XLU datapath control.

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Random little details

- The XLU also performs a load alignment function. This function bypasses the normal stage 1 mux operation, and is instead muxed into the datapath at the end of stage 1.
- While stages 1 and 2 use two sets of control signals, stage 3 uses three in order to handle sign extension. In addition, an additional pair of control signals is used to implement the shufflemux family of instructions. These additional control buses are shared between the high and low 64 bits of the datapath.

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- Stage 3 also performs zero/merge fill for some of the shift-related instructions. This is achieved by selecting shared column control signals with shared row selects, and using the result to determine whether the result should be taken from the main datapath or the fill bus.

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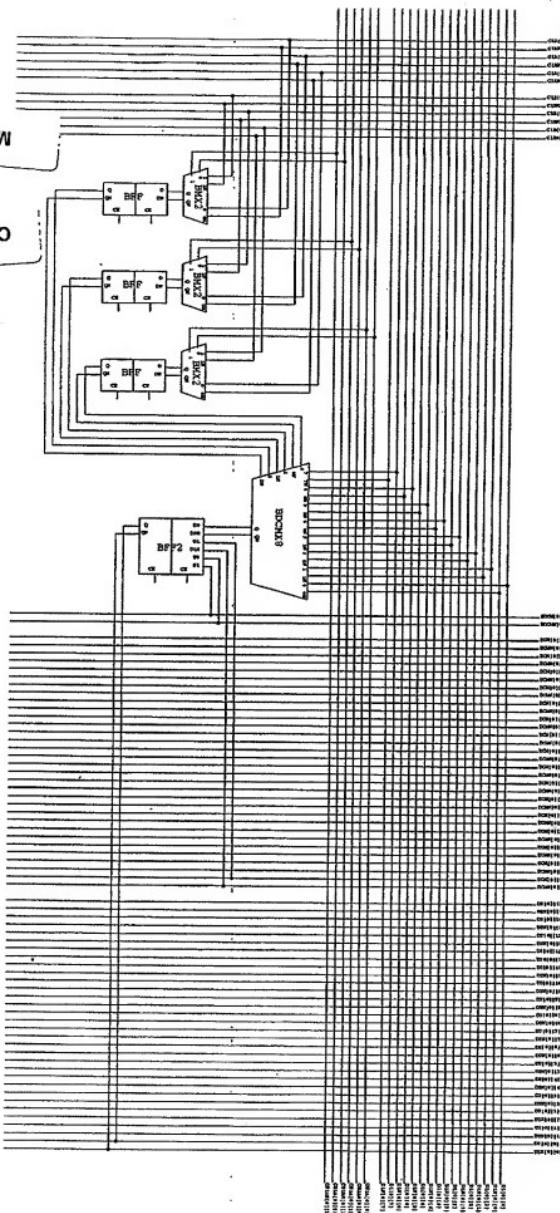
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BUDGET: TDK DATE: LAST MODIFIED:

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REV. NUMBER/EV

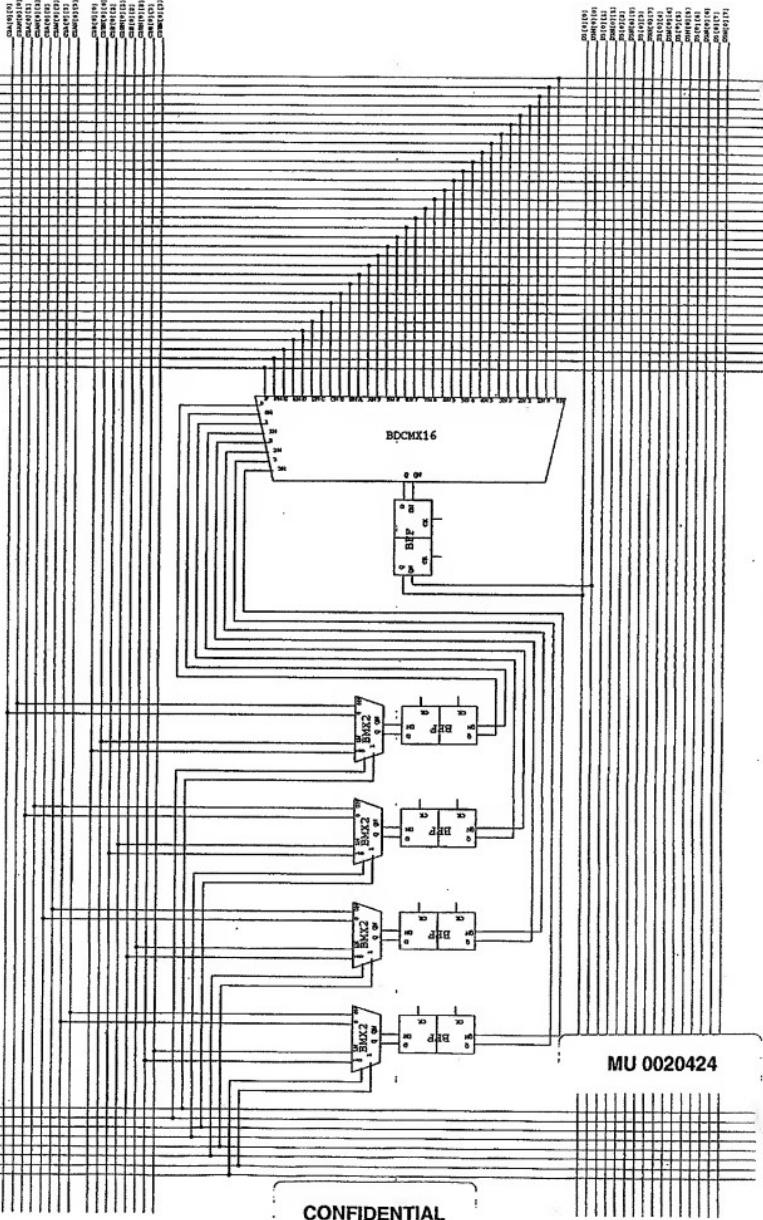


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DATE: LAST MODIFIED: 2021-01-20 BY: CHEN
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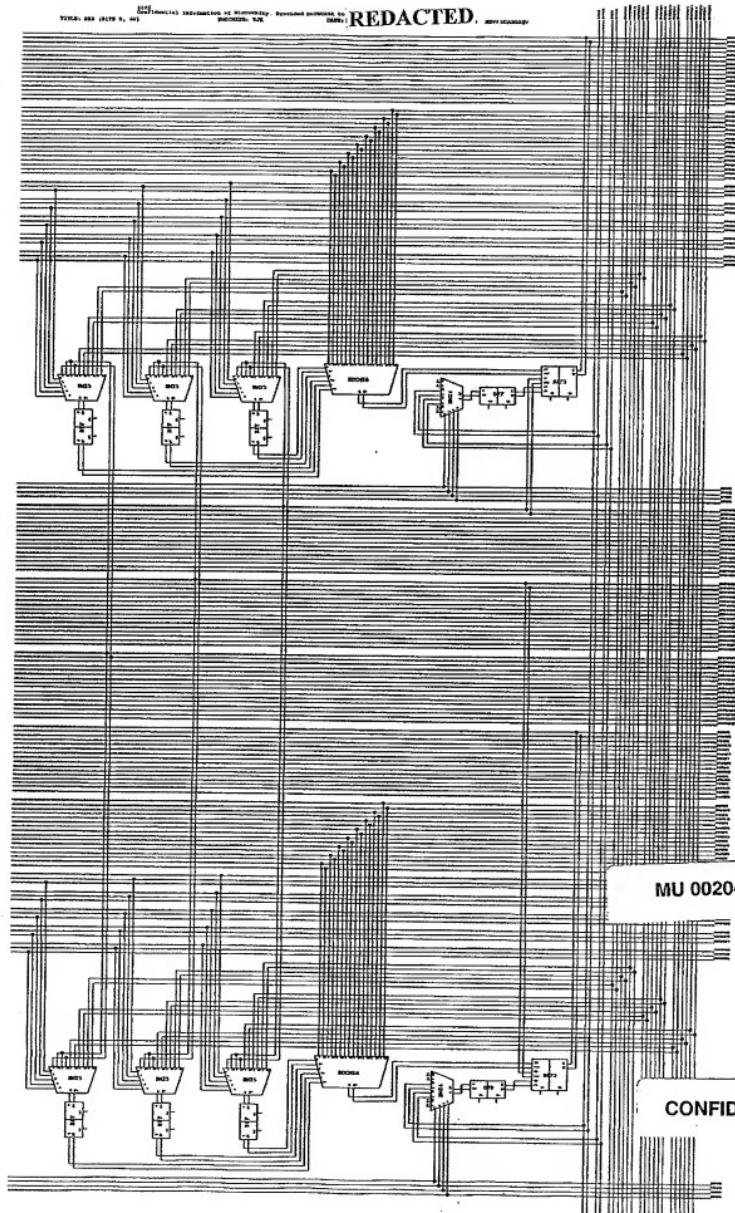
Stage 2, bit 0

TITLE: B92 (BIT 0)



Stage 3

6;10

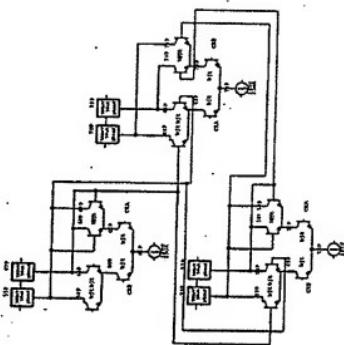
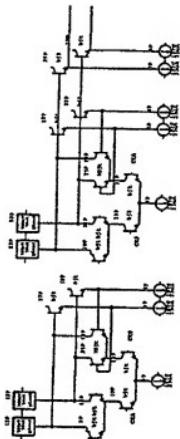
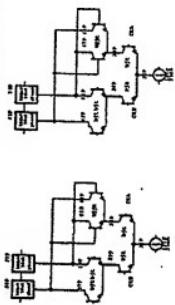


6;1 64

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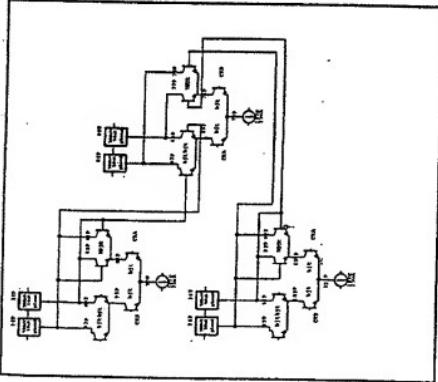
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FF CHANGES EVERY 800PS
-1600PS PERIOD CLOCK
000

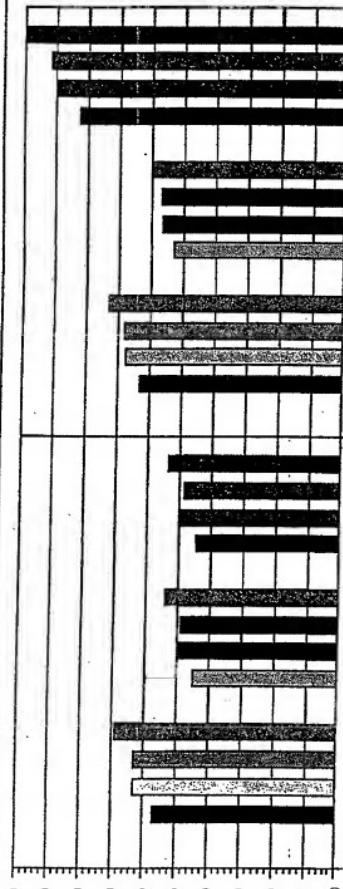
FF CHANGES EVERY 800PS
1600PS PERIOD CLOCK



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cond	Id (ps)	single in rise	multiple fall	d1/dc1 (ps/n)	d1/d0mV/d0Usa=k	d1/dc2	d1/dc1	d2/dc2	d1/dc2	c1	c2	lin	lin2	lin3	lin4
comp II=8/16	1	569	628	1.23	0.96	1.19	1.04	49H	49H	16	4	8	2		
	2	620	676	1.23	0.98	1.19	1.06	56H	49H	16	4	8	2		
	3	628	690					49H	99H	16	4	8	2		
	4	690	729					98H	99H	16	4	8	2		
no comp II=11	5	547	530	0.94	0.63	0.85	0.76	49H	49H	1	1	1	1		
	6	494	562	0.95	0.64	0.86	0.78	99H	49H	1	1	1	1		
	7	489	569					49H	99H	1	1	1	1		
	8	537	601					98H	99H	1	1	1	1		
o comp II=8/11	9	444	823	0.95	1.55	0.83	1.84	49H	49H	16	1	8	1		
	10	491	900	0.96	1.57	0.84	1.87	99H	49H	16	1	8	1		
	11	485	915					49H	99H	16	1	8	1		
	12	533	594					99H	99H	16	1	8	1		

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Circuit Speed/Power Optimization

- Motivation
- Timing-Driven Power Optimizer
- Simplified Delay Modelling
- Problems with Simple Models
- Improved Delay Modelling

Motivation

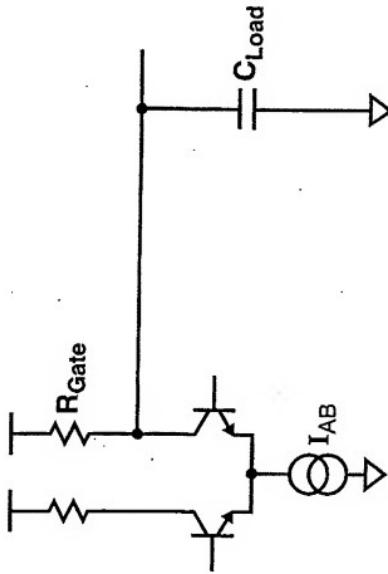
- Chip speed is limited by the slowest path
 - Need tuned drive strengths to guarantee speed
- Power of constant-current circuits is proportional to drive strength
 - Getting the most performance/Watt requires careful gate-level power tuning on a per-path basis
- Wire load dominates most nets and is indeterminate until after place & route
- Gate area is proportional to drive strength
 - Need iterative speed power optimization

Timing-Driven Power Optimizer (top)

Given a cycle time goal:

- Analyze the delay of every single-cycle path between flip-flops
- Determine the minimum-allowed signal level for unspecified paths
- Replace the gates in the path with ones which minimize area and power
- Try to make all paths critical!

Simplified Delay Modelling



$$T_{Delay} = T_{Int} + \log(2) * R_{Gate} * C_{Load}$$

Problems with Simple Models

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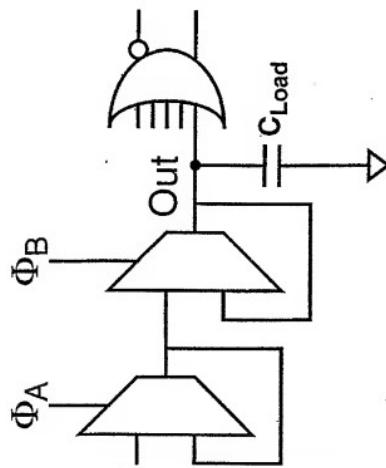
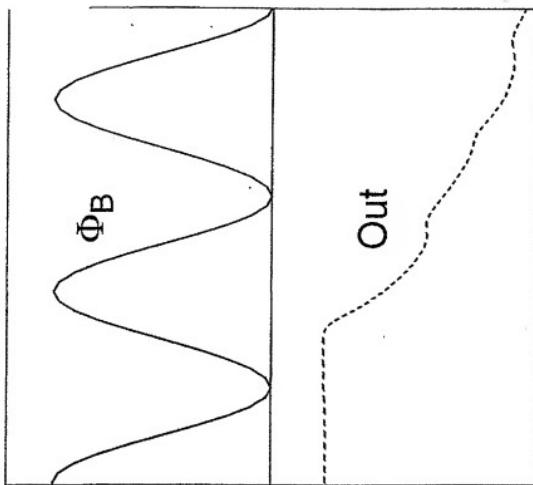
- Real gates are sensitive to input slope
 - Many cell libraries forced to use worst-case (i.e. slowest) input slopes to guarantee performance by overpowering
- Poor input slope increases both T_{int} and output slope
 - $0.7*R*C$ doesn't tell the whole story of load dependence
- Slope-dependent effects much worse for some gates
 - Wide OR gates with shifted references are especially bad
 - $\frac{-t}{RC}$
- Output waveforms do not always act like e^{-t}
 - Difficult to model slope with simple equations

Example - FF drives OR/NOR

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6



What are the delay and slope of the flip-flop output?

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Example - FF drives OR/NOR
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topf Delay Model

Gate delay is table-derived function of

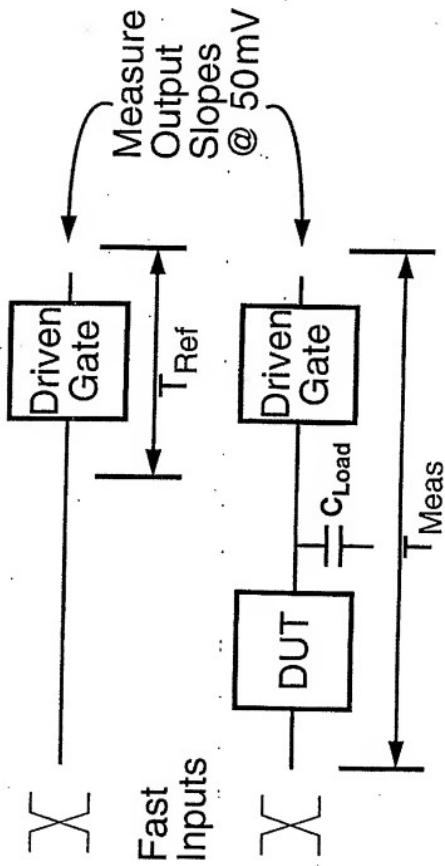
- Driving gate (i.e. which set of tables *topf* chooses)
- Output load capacitance
- Driven gate fanin (models impact of poor slope)
- Driven gate type (combinatorial or sequential)
 - Flip-flops assumed not to pass bad slopes, but require larger input transitions to satisfy latching constraints

Lump all slope-dependent effects upon delay of driving gate, but attempt to model it in context as best as we can.

top Delay Calculation

```
foreach net in path
    C_net = wire capacitance +  $\sum$ (gate input capacitance)
    Dly_tbl = f(driving_gate, driven_gate_type,
                driven_gate_fanin)
    Stage_dly = linear interpolation between delays of
                bracketing C_net entries in Dly_tbl
    Path_dly = Path_dly + stage_dly
endfor
```

Delay Simulation



Insertion delay model:

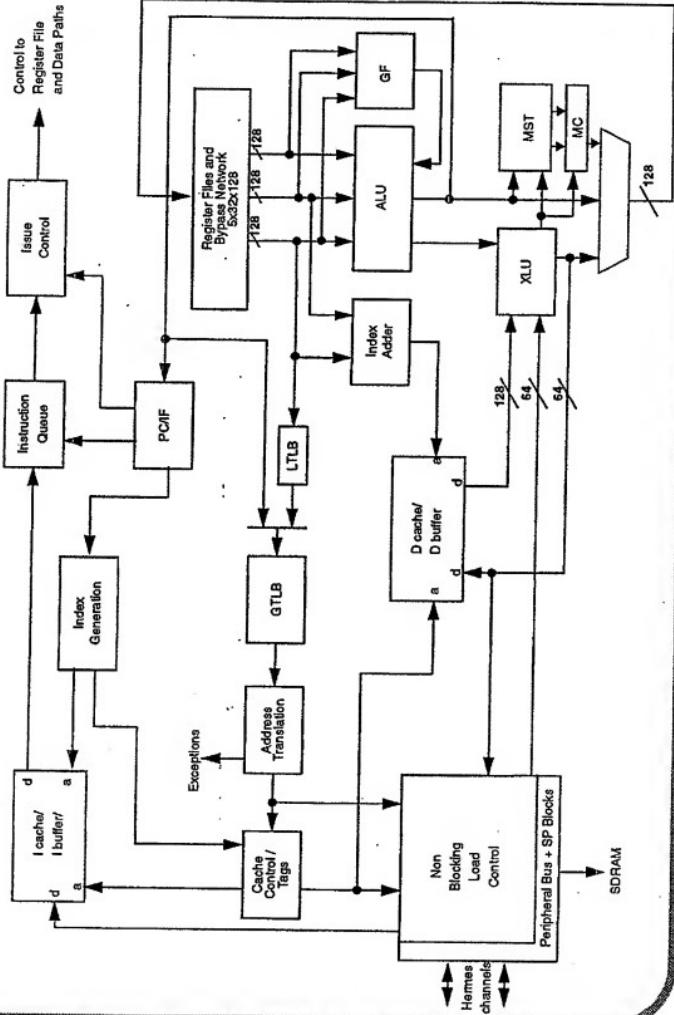
$$\blacksquare T_{Delay} = T_{Meas} - T_{Ref}$$

Delay Model Complications

- If driven gate is combinatorial, add measured delay to compensate for slowing its output slope
- If driven gate is sequential, its (slave) output slope is assumed to be independent of input slope, but T_{Meas} and T_{Ref} measured to 50mV differential at the latch feedback nodes
- Due to similarity of many gates, there are relatively few driven-gate combinations to simulate

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Euterpe Block Diagram

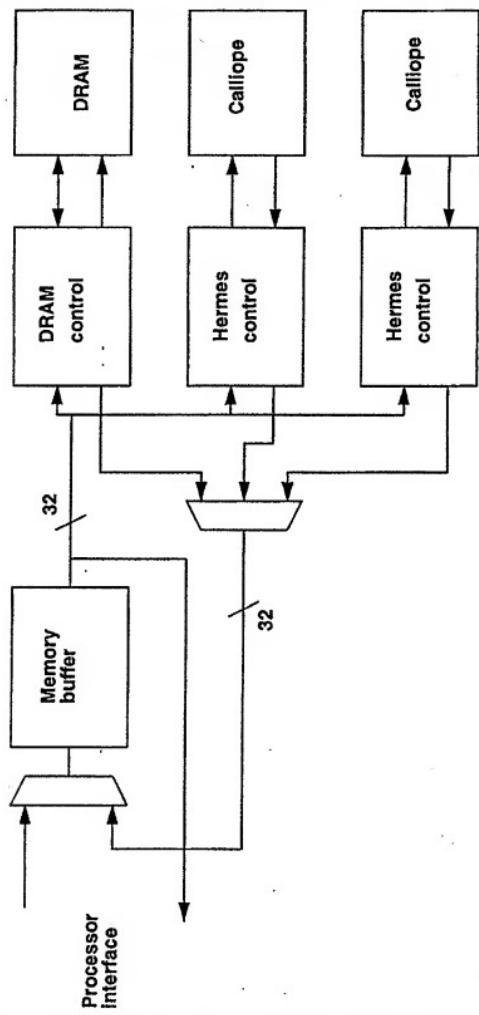


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Non-blocking Load Buffer

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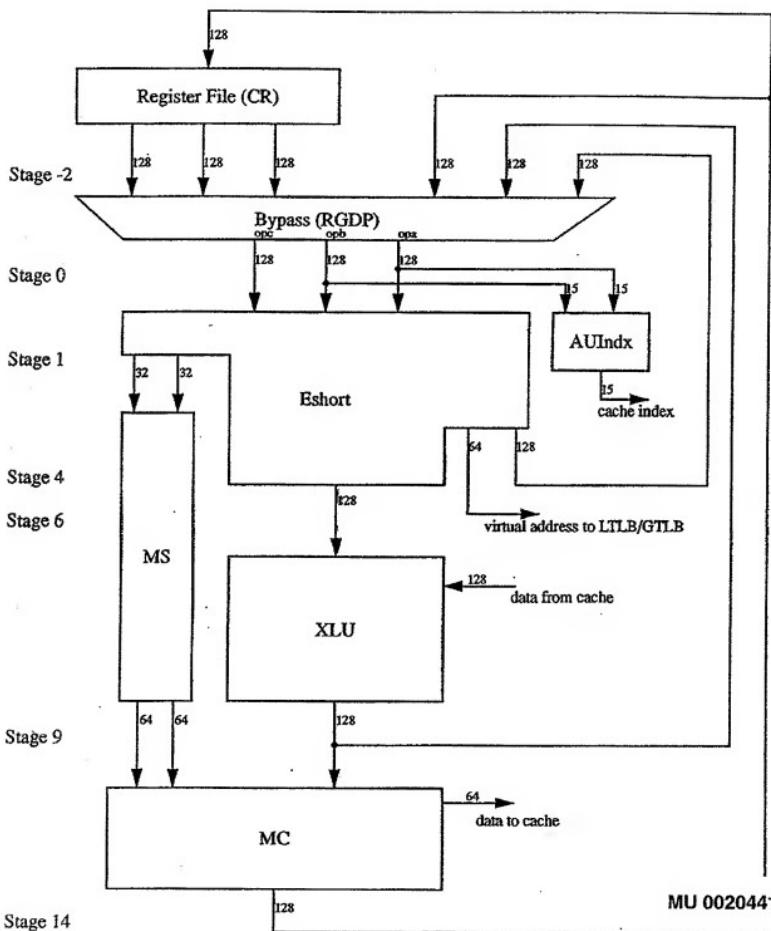


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Main Pipeline

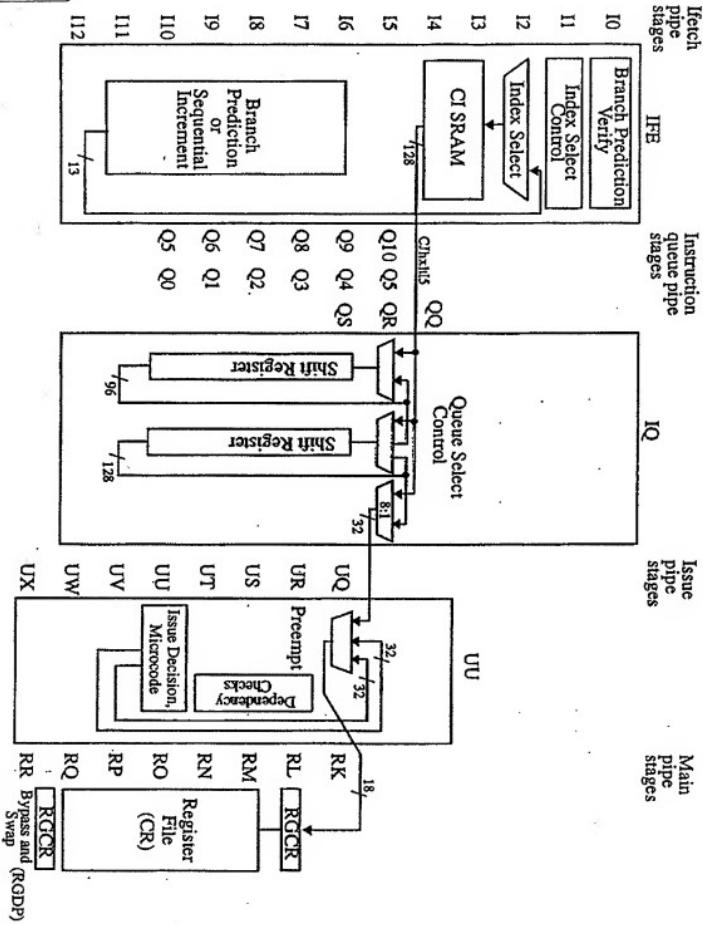


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R1

R0 EShort/AUIndx



Mask Data Processing

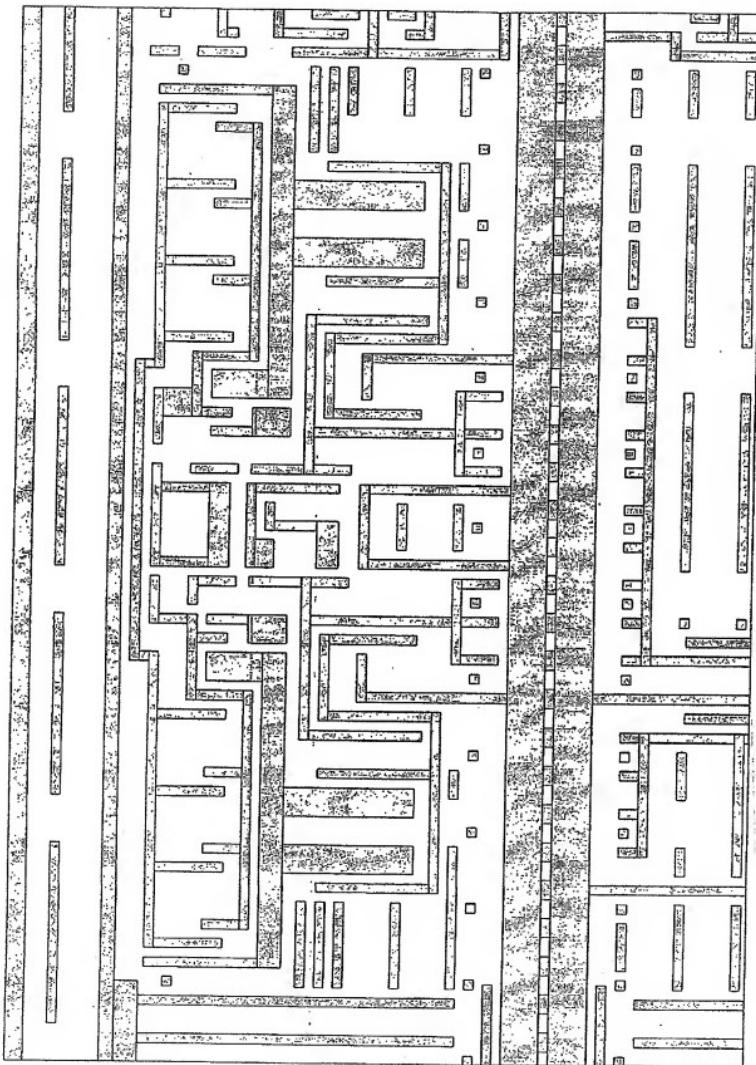
- In-house tool, "vlsimm" used for all back-end mask data processing.
- Derived layer synthesis (uses geometric AND, OR, grow/shrink etc.)
- Waftilization & perforation of metal layers to regulate pattern density.
- Computation of airbridge support structures.
- DRC checking of all derived data.
- Computation of Optical Proximity Correction (OPC) features: serifs, scattering bars, anti-scattering bars.
- Application of mask-vendor-specific feature biases.
- Direct output of MEBES pattern format, with automatic arrayed figure compaction.
- Post-fracture readback XOR check of pattern data.
- Complete MEBES job deck synthesis: composite reticle contains scribe frame, die patterns, bar code, fiducial/alignment marks etc.

Mask Data Processing

- Typical 28-layer reticle set contains around 6 billion rectangles.
- Figure compaction often achieves < 2 bytes per rectangle (uncompacted MEBES is 8 bytes per rectangle minimum).
- Fracturing is run on a 4-CPU SGI Challenge machine with 2GB of physical memory. An entire mask set can be fractured (including post-fracture DRC & XOR checks) in 2-3 weeks.
- 68 production reticle tapes issued to date.
- In-house pattern file viewer, "mebesview" supports instant examination of fracture results, automatic overlay of DRC/XOR flags, "pushbutton" hardcopy on PostScript laser printer or Versatec plotter.
- Key constraint: "vlsmim" processes Manhattan rectangles only - internal algorithms are all vertex-based for maximum speed. Process design rules disallow non-Manhattan geometry on all layers.

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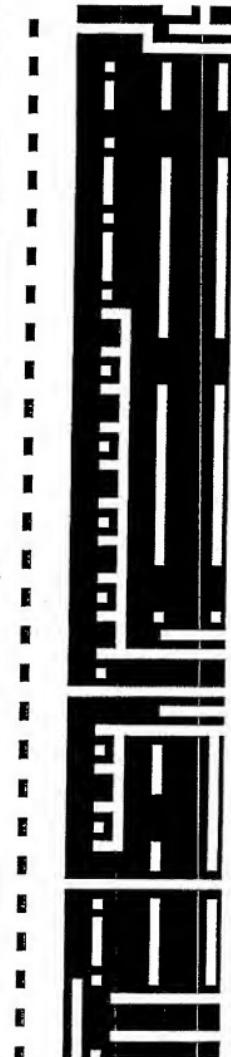
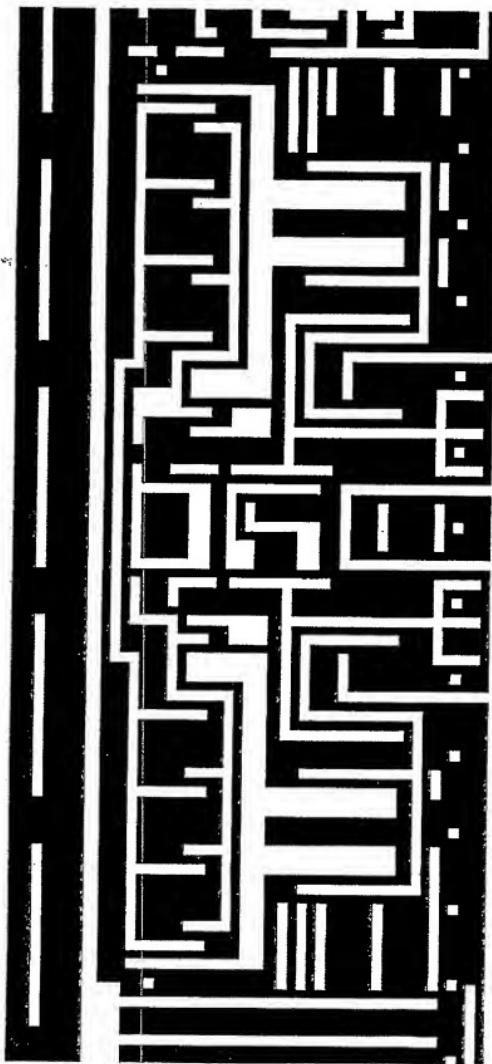
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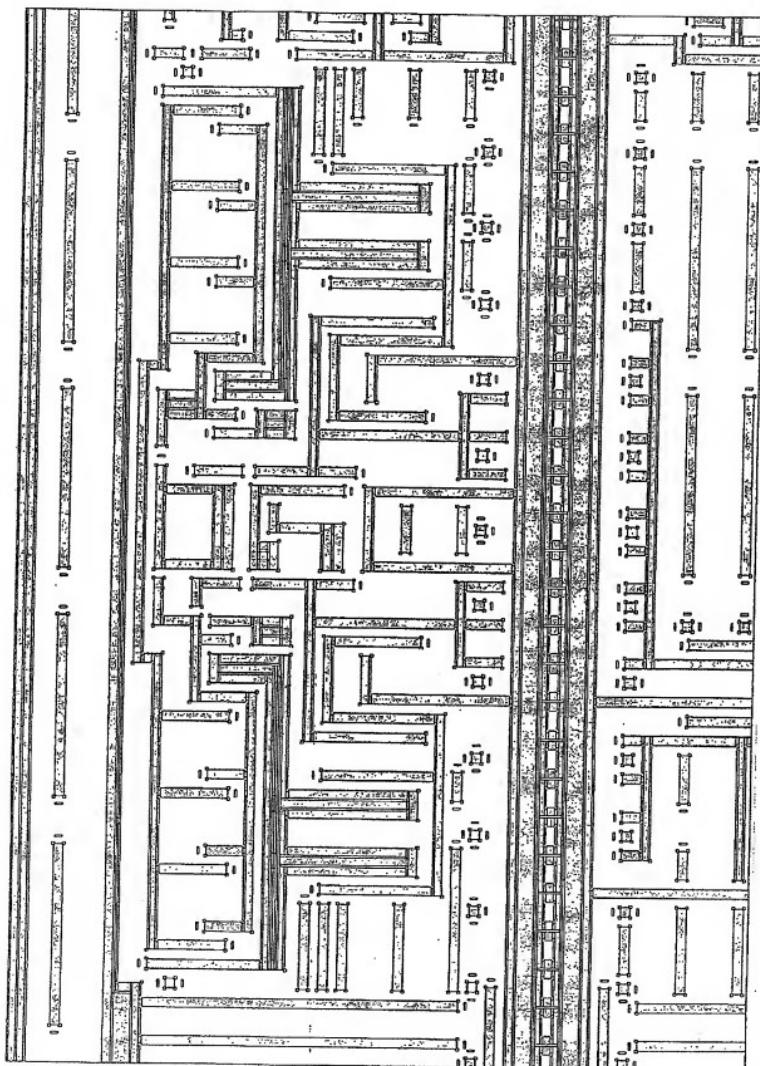
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MU 0020447



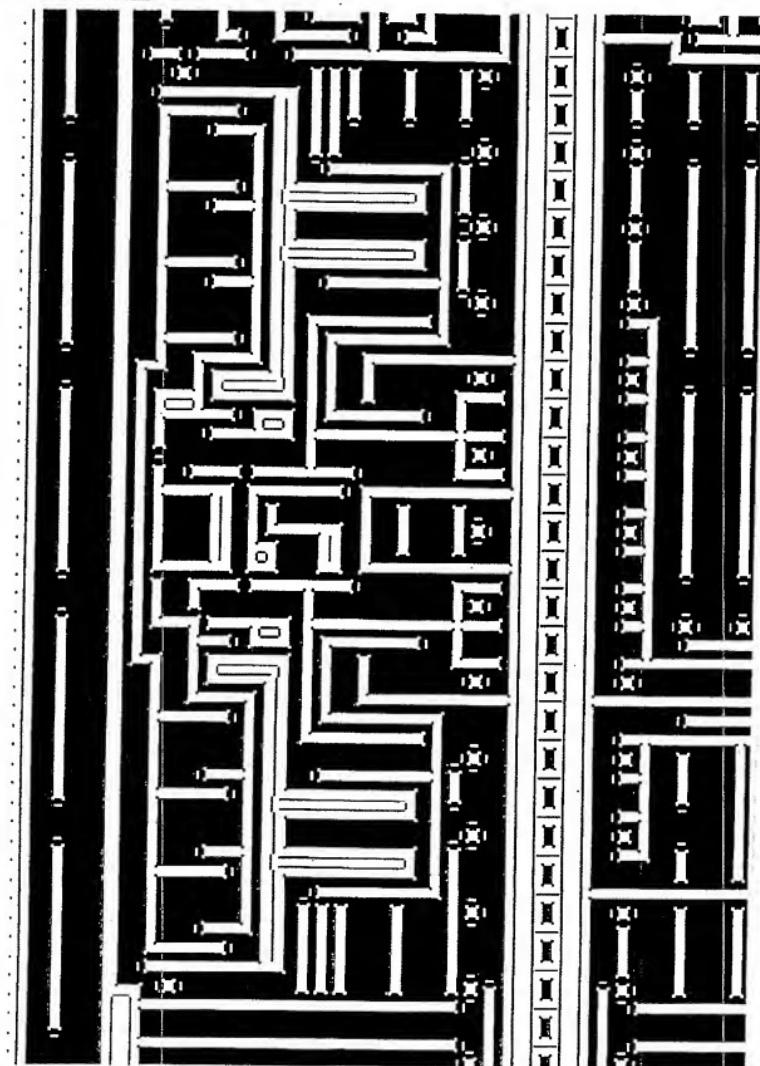
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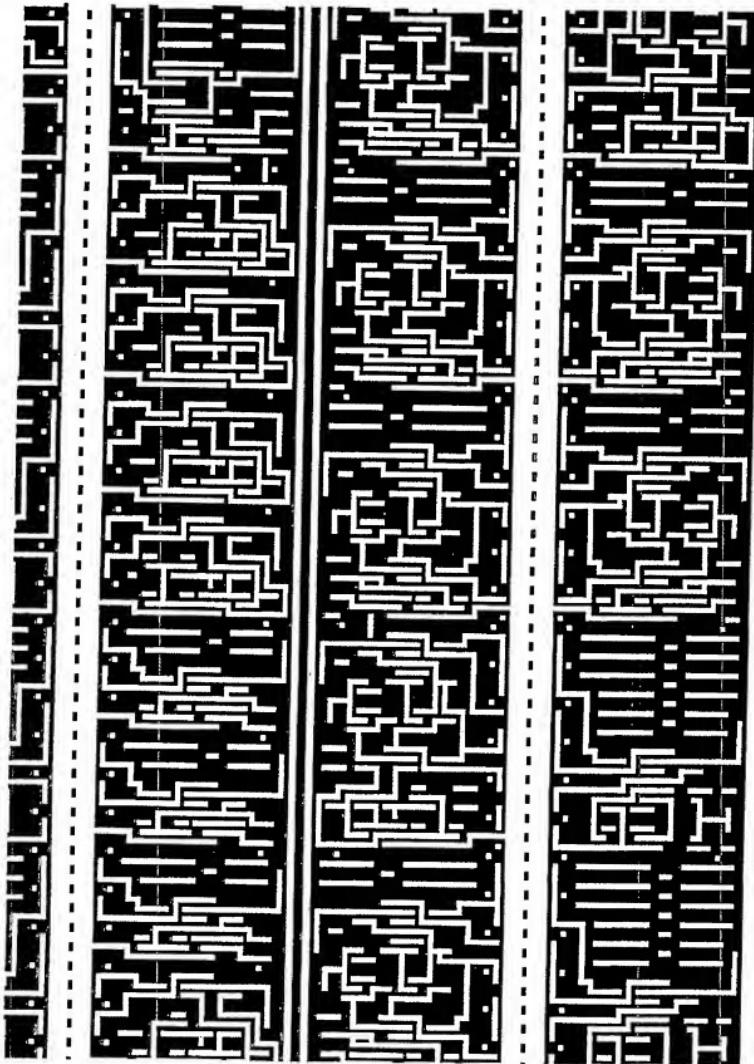
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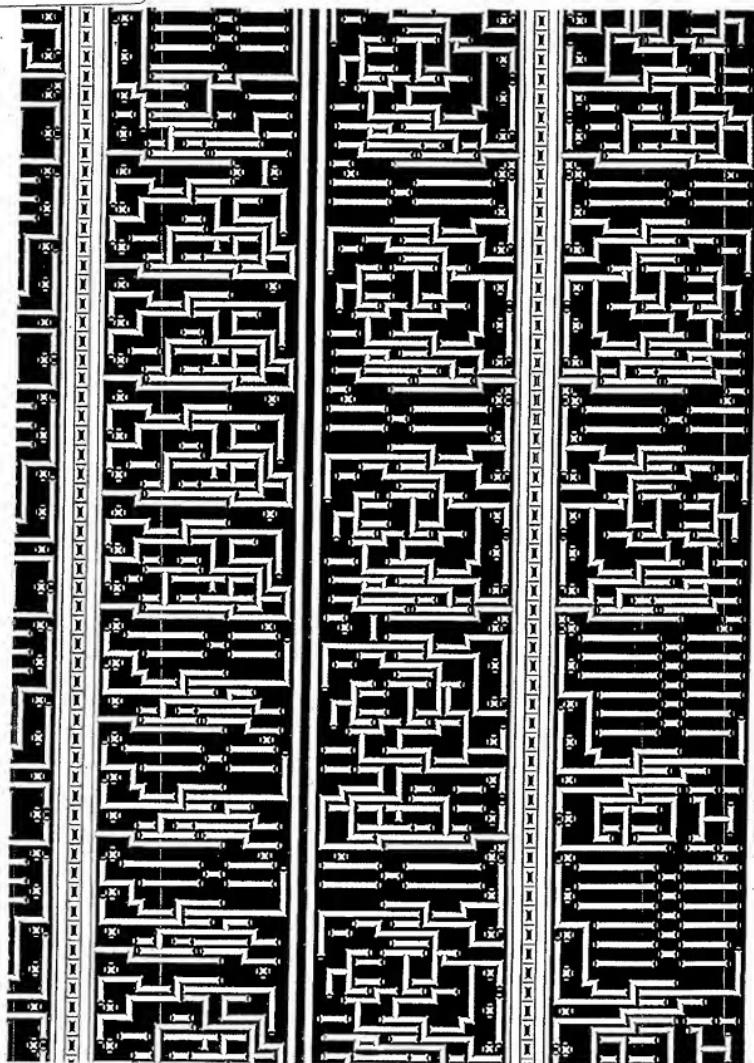


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WATER METALS
ORIGINAL METALS

METALS SURFACE PREPARATION
for METAL 4

